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13. ABSTRACT *(Maximum 200 words)*

In this report we detail the development of a GaAs based RTD that outperforms all other GaAs based RTD devices and many other devices in more exotic materials systems with >300kA/cm^2 peak-current density at 1.2V. This result was achieved by using a strained InGaAs well to increase peak current density while the valley current was kept low (>2:1 peak-to-valley ratio) by achieving smooth InGaAs / AlGaAs interfaces through the use of on-orientation MOCVD growth.

Circuits were designed and simulated using the measured parameters of the fabricated devices including an RTD driven sampling gate and an RTD based digital time delay. These two circuits form the basic building blocks of time-interval measurement and multi-channel sampling systems. A planar transformer was devised to allow the low ~1V output of the RTD to drive a 4 or 6 diode sampling bridge. Through the successful fabrication and circuit-simulation based demonstration of device performance, we have shown the feasibility of measurement instruments based on this technology.

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Introduction

As researchers throughout the world work to increase the speed of solid-state circuits for high-speed computing and signal processing, there is a persistent need for even higher speed measurement instruments. This is somewhat of a "chicken-and-the-egg" problem. The problem is compounded when the signal of interest is optical and high-speed electrooptic transducers are required as well.

Previously, the measurement problem was addressed with equivalent-time sampling oscilloscopes employing at first step-recovery diodes (SRDs) and tunnel diodes, then SRD-driven nonlinear transmission lines (NLTLs)[1] and tunnel diodes. The tunnel diode was used to provide a fast trigger circuit and the SRD/ SRD-driven NLTL was used to take a very quick sample (~6 ps) of the signal in question. Presently, the resonant-tunneling diode (RTD) is slated to replace the tunnel diode for triggering applications up to 100 GHz[2]. Although the hybrid SRD-NLTL-sampler approach works well for a few periodic signals, it does not handle large numbers of signals well, or signals that seldom repeat.

We have proposed to advance this RTD circuit and device performance to allow monolithic integration of a large number of samplers (~32) and process compatibility with photodetectors for optical signal applications. The ability to sample multiple signals on one chip makes possible a range of circuits and systems that require low skew and good matching between samples such as multichannel sampling oscilloscopes, transient digitizers and high-speed analog multiplexers.

In this report we detail the development of a GaAs based RTD that outperforms all other GaAs based RTD devices and many other devices in more exotic materials systems with >300kA/cm^2 peak-current density at 1.2V. This result was achieved by using a strained InGaAs well to increase peak current density while the valley current was kept low (>2:1 peak-to-valley ratio) by achieving smooth InGaAs / AlGaAs interfaces through the use of on-orientation MOCVD growth.

Circuits were designed and simulated using the measured parameters of the fabricated devices including an RTD driven sampling gate and an RTD based digital time delay. These two circuits form the basic building blocks of the multi-channel sampling systems listed above. Through the successful fabrication and circuit-simulation based demonstration of device performance, we have shown the feasibility of measurement instruments based on this technology.

Summary of Key Phase I Results

We have found that GaAs integrated circuits based on RTDs, Schottky diodes, and passive transmission line elements can provide dramatic speed improvements when applied to waveform sampling systems such as transient digitizers or sampling oscilloscopes. The specific achievements include:

1. A GaAs based GaAs/AlGaAs/InGaAs/AlGaAs/GaAs RTD structure that achieves greater than 300kA/ cm^2 peak current density at 1.2 V: a result only exceeded in much more exotic materials systems. Although the device was not fabricated in a low-parasitic process for high-speed testing, simulations based on calculated device capacitance and the measured I-V curve show that this device should switch 1V in about 3ps. An optimized design is expected to approach 1ps. The measured I-V curve is shown in Figure 1.

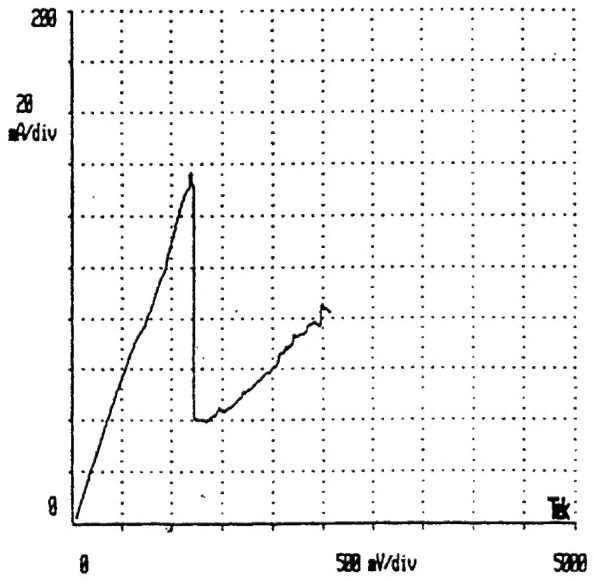

*Figure 1: Measured I-V curve for a 6*6 μm^2 device at room temperature.*

The key to success with this structure was achieving smooth interfaces between the strained and lattice matched layers through the use of MOCVD growth with "on-orientation" GaAs substrates. This work is detailed in Appendix A.

1. A planar transformer capable of unbalance to balance conversion and transforming pulses to provide sufficient drive voltage for a Schottky diode sampling bridge. Scale model results indicate a 1.8 x increase in voltage with rise-times that scale to < 1ps (Figure 2).

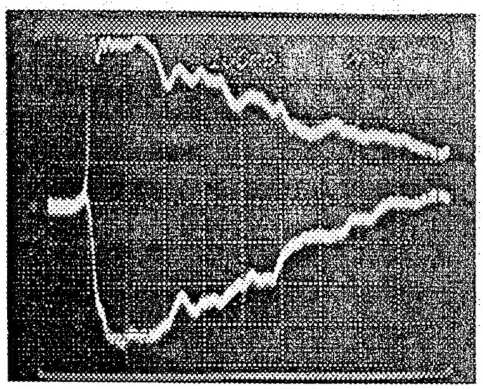

Figure 2: 2x attenuated balanced output of planar transformer 400:1 scale model. 100mρ / vertical division, 2 ns/ horizontal division.

2. An RTD based digital delay line for sequential strobing of sampling bridge arrays. This circuit was demonstrated by circuit simulation using realistic RTD models based on measured I-V curves and calculated device capacitance for non-optimized devices.

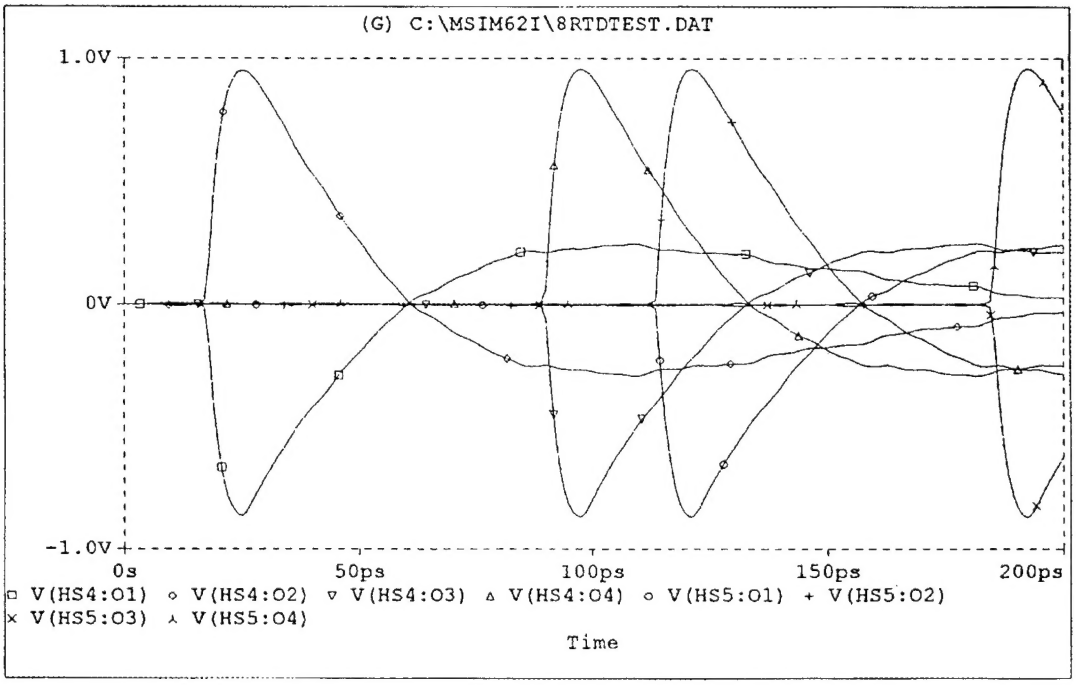

Figure 3: Simulated output of an RTD based digital delay line driving planar transformers. Differential outputs 1, 4, 5, & 8 are shown. The top 200 mV will turn on the sampling diodes with a width of 6-10 ps from this simulation.

Summary of Phase I tasks

The contractor will study and demonstrate the feasibility of using resonant tunneling diodes (RTDs), nonlinear transmission lines (NLTLs), and monolithic-sampler technologies to make picosecond-resolution time-interval measurements at rates up to 2 GHz. These studies shall include, but not be limited to:

a. Model the operation of RTDs designed for growth by metalorganic chemical vapor deposition (MOCVD), less than l0 ps, greater than 1 V switching, stable and reproducible threshold, photonic switching, process compatibility with Schottky and photo-detecting diodes, and high-reliability.

b. Model and optimize performance of the various RTDs in the timing circuits described in the proposal, as well as more refined circuits, to show circuit function and dependence on RTD parameters using theory, numerical simulation, and scale models.

c. Estimate the accuracy of the timing circuits in the following applications: time-jitter measurement in optical networks, time-of-flight mass spectroscopy, and photon counting in picosecond fluorescence experiments.

d. Grow an RTD structure by MOCVD and compare its performance to that of the models described above.

e. Demonstrate photonic switching

Process Compatibility of RTDs and Schottky diodes

Before considering sampling circuits based on Schottky diodes and RTDs, it must first be shown that these elements are process compatible. Actually, this has already been demonstrated by Miura[3] for the InP based RTD, Rodwell[4] for the Schottky-collector RTD and by Chow[5] for the RIT RTD. The addition of the Schottky diode requires an additional low-doped layer to be grown on the surface and an extra mask to pattern the Schottky. Ohmic contact is made to the buried Schottky/RTD connection with a non-critical, self-aligned etch of the low-doped Schottky surface to an underlying heavily doped contact region.

If the Schottky diode is to be used as a photodiode, the process is the same except the Schottky metal must be semi-transparent. Very thin gold has been used successfully for room-temperature applications, but is problematic at the elevated temperatures that result from operation of RTDs nearby. The "metal" then must be both transparent and stable at high-temperature. Indium-tin oxide has been shown to have these characteristics but has higher sheet resistance and would result in some compromise of photodiode speed. Alternatively, an interdigitated structure could allow light in, but would require sub-micron lithography to achieve high-speed operation.

RTD Circuit Optimization

The fact that the RTD has only two terminals is a source of both simplicity and complexity. It is relatively simple to make an effective RTD circuit model for numerical circuit simulation since it's behavior is nearly completely defined by its current-voltage (I-V) relationship, junction capacitance, and parasitic resistances. The I-V curve can be measured if provisions are made to prevent oscillation in the negative differential resistance region and the parasitic elements can be simply calculated with reasonable accuracy. Greater sophistication can be applied to speed convergence, or aid in design[6, 7] if necessary.

However, the lack of a control terminal makes the RTD quite difficult to design a circuit around. The various circuit input and output terminals are often tied directly together, resulting in a circuit with load dependent performance and no isolation between inputs. Another disadvantage of the RTD is low voltage operation. Low voltage and high-speed typically go together in semiconductor devices and the same holds true for RTDs. This fundamental limit in majority carrier devices is simply because carrier transit time and break-down voltage scale linearly with the critical device dimension for a given breakdown field strength and saturated carrier velocity. In bulk GaAs, this number is about 4V breakdown for every picosecond of transit time. Considering surface breakdown and allowing some margin, 1 ps devices shouldn't be expected to function above 3V. Since our simulations show that peak-current voltages much below 1V would be difficult to achieve with a strained well, the maximum conceivable voltage swing for this technology is 2V.

The primary building block for the high-speed measurement instruments proposed here is the four diode sampling bridge (Figure 4). The sampler's drive voltage requirement arises from the need to keep diodes D1-D4 off over the allowed signal voltage range when a sample is being held, and to keep them on when a sample is being taken. For the hold state, V_a must be more negative than the most negative allowed input signal voltage, V_{in} and must swing to a voltage greater than the most positive V_{in} plus one diode drop and the IR drop across the series resistor. The total V_a swing is then $2V_{in}+V_j+I_{on}R$. The total differential voltage swing, $V_a - V_c$ is then $4V_{in} + 2V_j + 2I_{on}R$. For a modest 0.2V maximum input voltage, diode on resistance of 25 ohms (I_{on}=1mA), series resistance of 100 Ω, and a diode drop of 0.8V, the differential drive requirement reaches 2.45 volts. Now add to this some margin to allow for ringing and pulse broadening on the base of the strobe pulse, and the requirement is 3V.

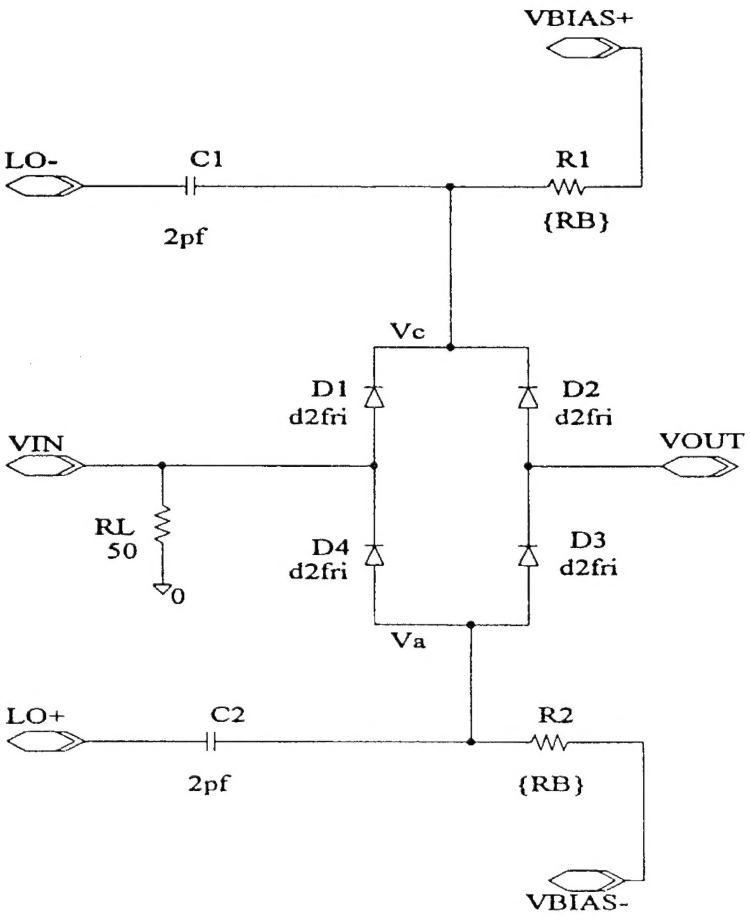

Figure 4: 4 diode sampling bridge

This is a bit of a stretch for an RTD that fails at 3V. The main task then is designing a sampling circuit that can work with a <2V driver. There are three possible ways to approach this: voltage transformer, reduced drive requirement sampler, and ganged drivers. Each of these approaches is feasible and is detailed below, but the ganged driver triggered by a transformer appears to be the most practical (produces the highest voltage).

Sampling Circuits

The Planar Voltage Transformer

Normally transformers are not useful for high-speed pulse circuits because it is impossible to make a traditional transformer with a fast enough response. However, transmission line transformers have no intrinsic upper frequency limitation. These structures involve splitting the incident field into two higher impedance modes and then adding them back together in a higher impedance transmission line. The simplest structures result in 2X

more voltage in a 4X higher impedance. This is fine for driving a sampler which typically has a very high impedance.

Although transmission line transformers have been around for some time, we are not aware of any monolithic versions that are compatible with GaAs processing. Our transformer is illustrated in Figure 5. The 50 Ω input coplanar waveguide is connected to two 100 Ω coplanar strip lines in parallel. These coplanar strip lines are recombined in series after a length, L. If the center point of the series combination is connected to ground, the transformer output will be balanced. This simple explanation assumes that the coplanar strips can be treated separately, and that common mode signals do not propagate on the coplanar lines. Actually, there is some coupling between the lines. This is reduced by using asymmetric coplanar strips with a "ground" strip isolating the signal lines and separating the lines as much as practical. The second assumption is the most damaging in that it is the common-mode propagation that limits the useful frequency range of this device. Obviously, a dc voltage can't be sustained across the structure, and so the output will return to zero after some number of common-mode reflections traverse the structure. So, the length of the structure determines the pulse-width that can be passed, or similarly, the lower frequency limit.

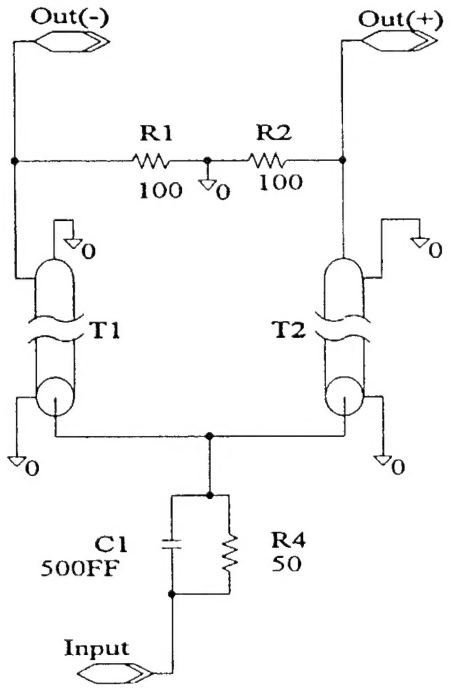

Figure 5: Transmission line transformer

The high-pass nature of the transformer can be exploited to turn a step signal into an impulse, or it can be designed to pass an impulse formed by other means. In either case,

the transformer can provide a well matched input impedance at all frequencies with the addition of a series resistor and a "speed-up" capacitor. High-frequency signals, are connected to the transformer through the capacitor while low frequency signals are dissipated in the resistor.

Mmicad software from Optotek was used to optimize the structure. The strip-lines were modeled as asymmetric coupled microstrip. This model is good because it handles both the asymmetry and the two main propagating modes, but doesn't handle the case with no ground plane. In practice, the performance is not dramatically effected by the presence or absence of a ground plane providing the strip widths and gaps are much less than the substrate thickness.

After optimizing for minimum reflection, a scale model of the transformer was built on 1" thick Stycast Hi-K material with ε_r=12 (Figure 6). For eventual substrate thickness of 125 μm, this is a 200x scale model. The strip widths were 0.0625" and 0.25" with a 0.130" gap. Fabrication was by hand so accuracy was about 0.025". The 8" long structure showed flat top pulse transmission for approximately 4 ns as shown in Figure 7. This corresponds to an effective dielectric constant of 8.7 for the common mode. A scaled structure fabricated on 125 μm thick GaAs would be 1mm long and function for pulses up to 20 ps wide.

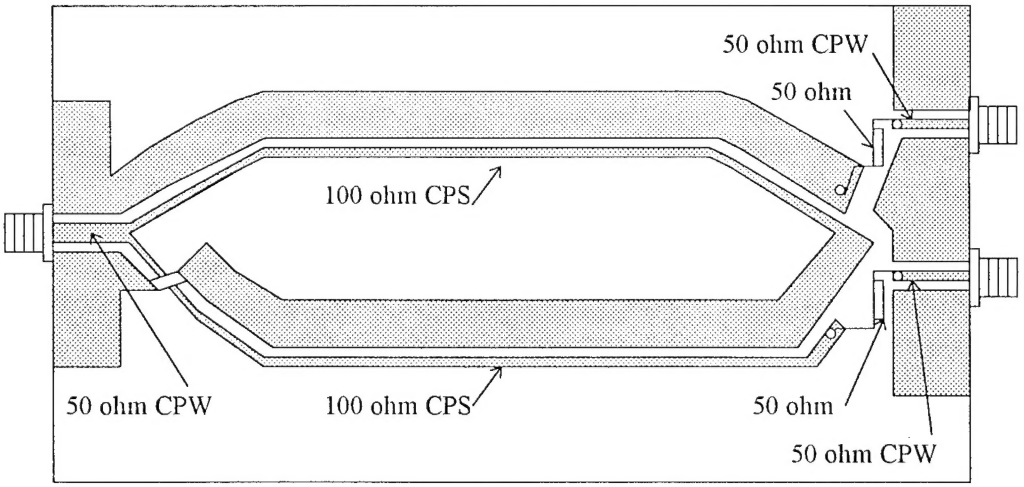

Figure 6: Drawing of transformer scale model shown connected for balanced output and attenuated for display on a 50 Ω scope.

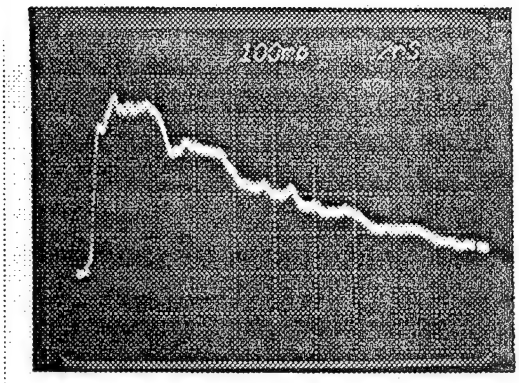

Figure 7: Output of scale model attenuated 4:1 and connected for single ended operation.

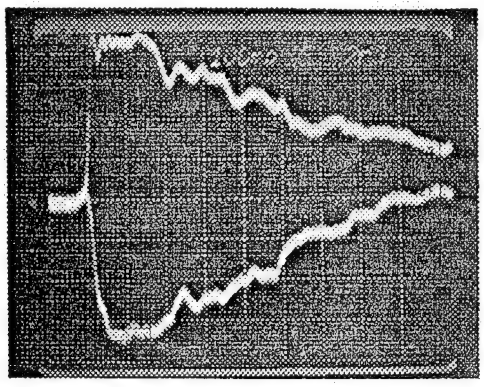

Figure 8: Output of scale model transformer after 2x voltage division to provide proper 200 Ω balanced termination when driving a 50 Ω scope.

To test performance as a balun, the output of the scale model was connected as shown in Figure 6. The two 50 Ω outputs with series 50 Ω resistors are connected in series to provide the correct termination. In practice, the loads should be 100 Ω on each side to avoid voltage division. Results are shown in Figure 8. The balun function is clearly evident, although the negative side shows a slightly longer rise-time and the amplitude is only 80% of the theoretical value. The longer rise-time is probably because the negative side is connected to the larger strip that has greater dispersion and loss into the substrate. The larger strip is approximately 1/2 wavelength wide at the 3-dB frequency of the input signal. The resulting 300 ps rise-time corresponds to 1.5 ps in the scaled device and is acceptable. The amplitude loss is difficult to relate to the scaled structure due to the effects of metal thickness, adhesive, and line width variations that do not scale and was not investigated further.

Ganged Drivers

The idea of ganged drivers is to switch two or more RTDs at the same time to achieve an increase in drive voltage. This is facilitated by the fact that a balanced

sampling bridge requires both positive and negative pulses. If separate RTD's are used for the two sides, only half the voltage is required of each. This approach assumes that the trigger recognition is being accomplished by a separate circuit that triggers these RTD's at precisely the same instant. Since the two RTDs are producing opposite polarity pulses, opposite polarity triggers will be required as well. This is a natural application of the monolithic transformer. Even if the transformer can't boost the RTD voltage sufficiently to drive the bridge directly, it can provide opposite polarity simultaneous trigger pulses for the two bridge-driving RTDs.

A schematic diagram of this approach is shown in Figure 9. The first transmission line transformer functions as a balun because of the symmetrical load and triggers RTDs D2 and D3. The next set of transmission lines function as single ended step up transformers. The positive and negative outputs driving 200 Ω loads are plotted in Figure 10. The differential pulse amplitude is substantially larger than the required 3V.

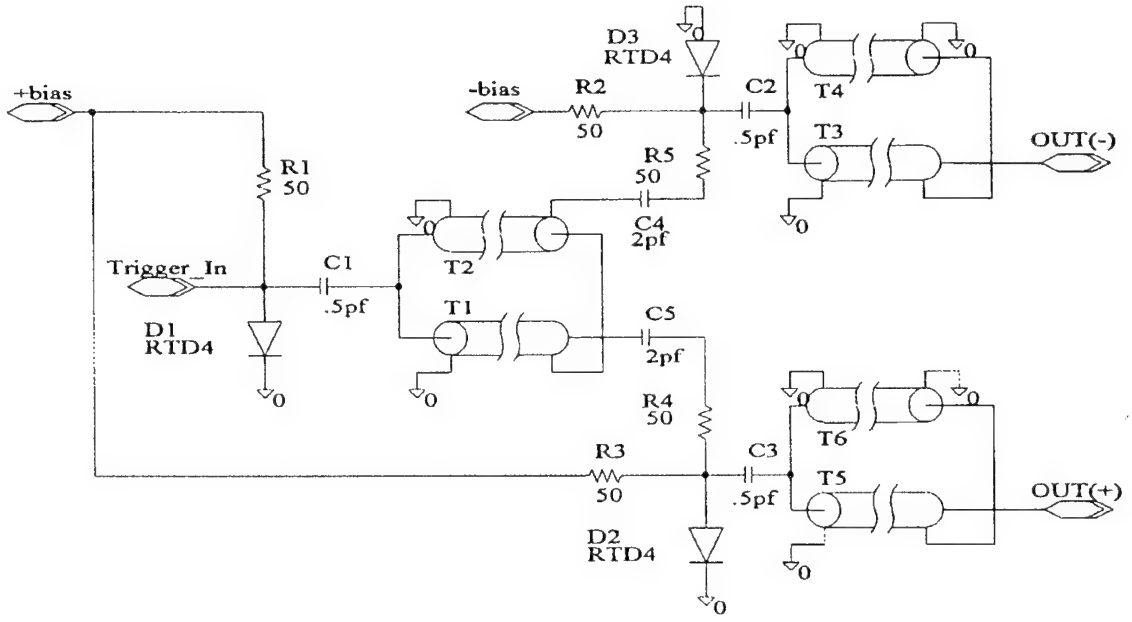

Figure 9: Schematic diagram of sampling system using ganged drivers.

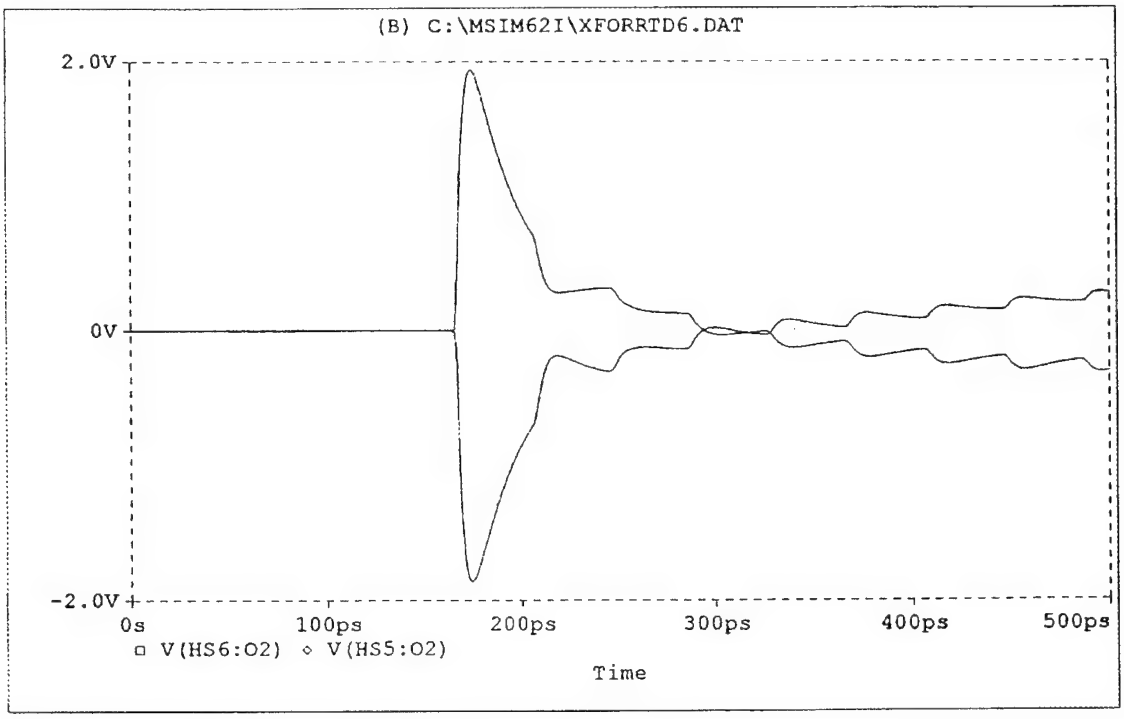

Figure 10: Outputs of ganged driver circuit. Peak differential voltage is nearly 4V.

Reduced Drive Voltage Sampler

If the first two techniques don't provide enough voltage for the number of samplers to be driven, it is possible to reduce the drive voltage requirement. However, this is the least desirable option as there is almost always a trade-off to be made for reduced drive voltage. The most desirable method from a circuit point of view is to reduce the Schottky diode turn on voltage, possibly in a manner similar to Miura[3] or Chow[5], but this adds both epitaxial-growth and process complexity. The easiest method from a manufacturing standpoint is reduction in the number of series connected diodes to be switched. This reduces the requirement to 2.6V - 0.8V = 1.8V, just inside the RTD's reliable range of operation.

The price to be paid here is that the sampled output voltage contains an offset related to the strobe pulse height and so a parallel sampler is required to provide the value to be subtracted off (Figure 11). This creates an additional source of error due to the need of an analog or digital subtraction. At these low drive levels, the sampler will be somewhat nonlinear making the offset correction even more difficult. The conclusion is that reducing diode sampling bridge drive requirement below 2.6V results in unacceptable compromises. Fortunately, the ganged driver/ monolithic transformer approach can easily achieve 2.6V with only the penalty of increased circuit complexity and recovery time. A three terminal device would be required to eliminate the transformer and achieve ultrafast recovery time.

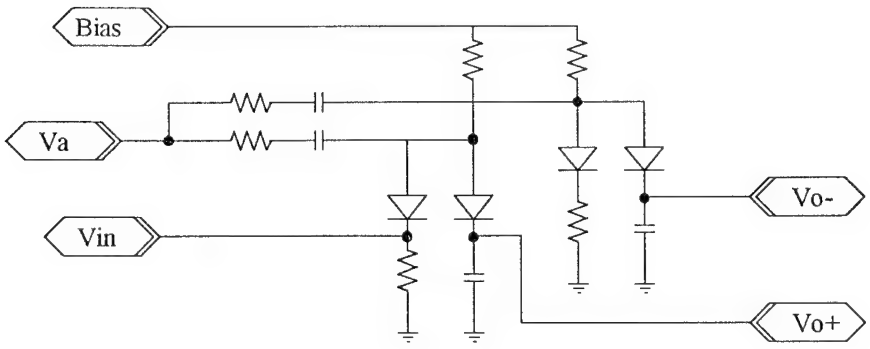

Figure 11: Reduced drive voltage sampler with provision for measuring offset

The RTD Digital Time Delay

Due to the finite recovery time of the sampling circuits investigated and the difficulty in processing data at rates above 1 GHz, it became clear that it would be useful to have a multiplexed array of samplers that could sample and hold the data until it could be processed. Large numbers of individual samplers rapidly become unwieldy due to the large number of high-frequency connections for input and local oscillator signals and the desire for channel to channel isolation. On chip multiplexing reduces the risk of this approach by reducing the number of bond-wire connections. The local oscillator port is the most difficult due to the high amplitude and speed of these signals. This port is also the easiest to multiplex because isolation and detailed signal integrity are less critical. A new circuit was devised to accomplish this task.

The requirement for the new circuit is to strobe each of a number of samplers in turn after a fixed delay. It was found that a digital time delay shown schematically in Figure 12 could be implemented in a simplified form of RTD logic. Such logic gates have been analyzed in great detail first for tunnel diodes[8]. The one advantage of the tunnel diode was that it could be easily integrated with the "back" diode which is basically a tunnel diode with very low peak current and extremely low turn-on voltage in the reverse direction. The back-diode is a natural input element for a logic gate (Figure 13) because it provides isolation between inputs and some input-output isolation. Although recent work shows great promise[5], RTDs are not readily integrated with a such a diode.

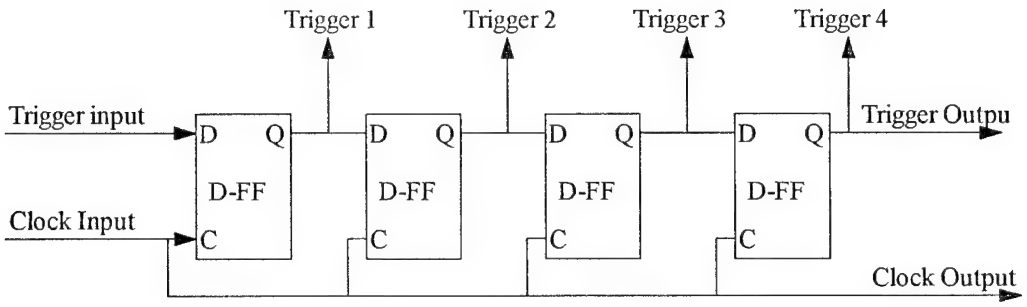

Figure 12: Desired digital time delay function

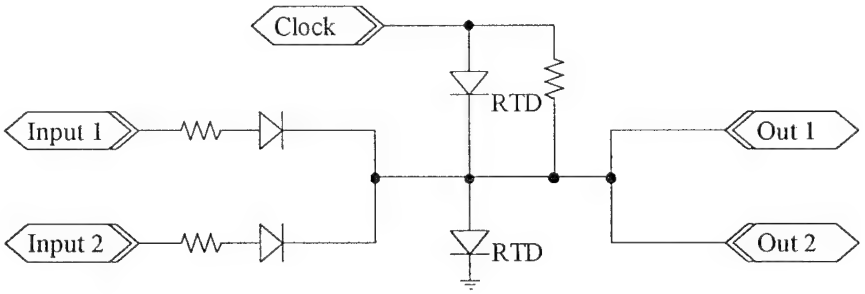

Figure 13: Tunnel or RTD logic gate with low-turn-on voltage input diodes to provide isolation.

A disadvantage of logic gates as shown in Figure 13 is that the input signals can't reset the RTDs. Only one logic operation can be accomplished per clock cycle. This requires subsequent gates to be synchronized so that they are not reset at an inappropriate time.

Fortunately, the circuit of Figure 12 does not require input isolation when used for the special purpose of triggering samplers. Therefore, it is possible to implement the delay circuit using only resistors and RTDs (Figure 14). This circuit is also easy to synchronize requiring only a bi-phase clock. Very small area RTDs are desirable for this application due to the large clock fan-out required. The device parameters used to simulate these circuits are listed in Table 1.

Table 1: RTD simulation parameters

Parameter	*RTD2*	*RTD3*	*RTD4*
Area, μm^2	9	4.5	18
Capacitance, pF	0.069	0.034	0.140
Peak Current, A	0.034	0.017	0.068

The simulation result shown in Figure 16 uses RTD2 and RTD4 which are ¼ and ½ the area respectively of the device actually measured in Figure 1.

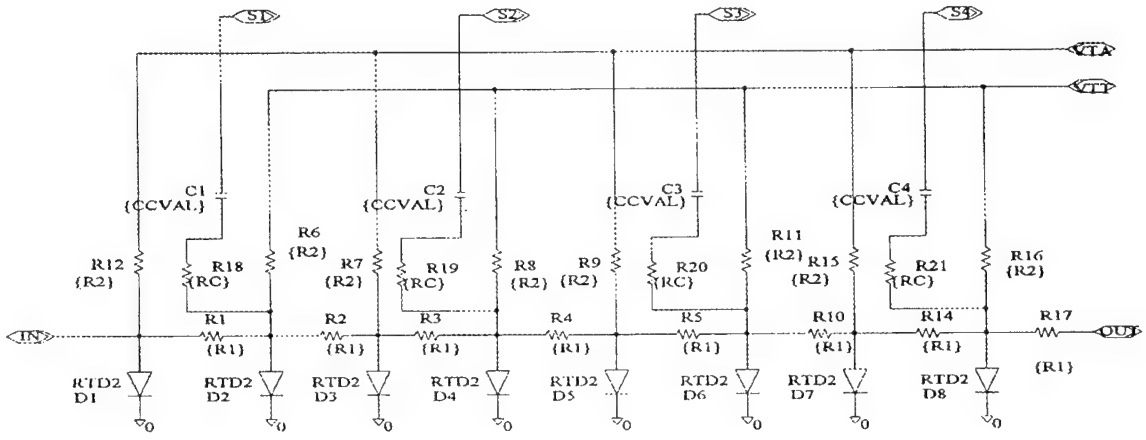

Figure 14: RTD based digital time delay circuit

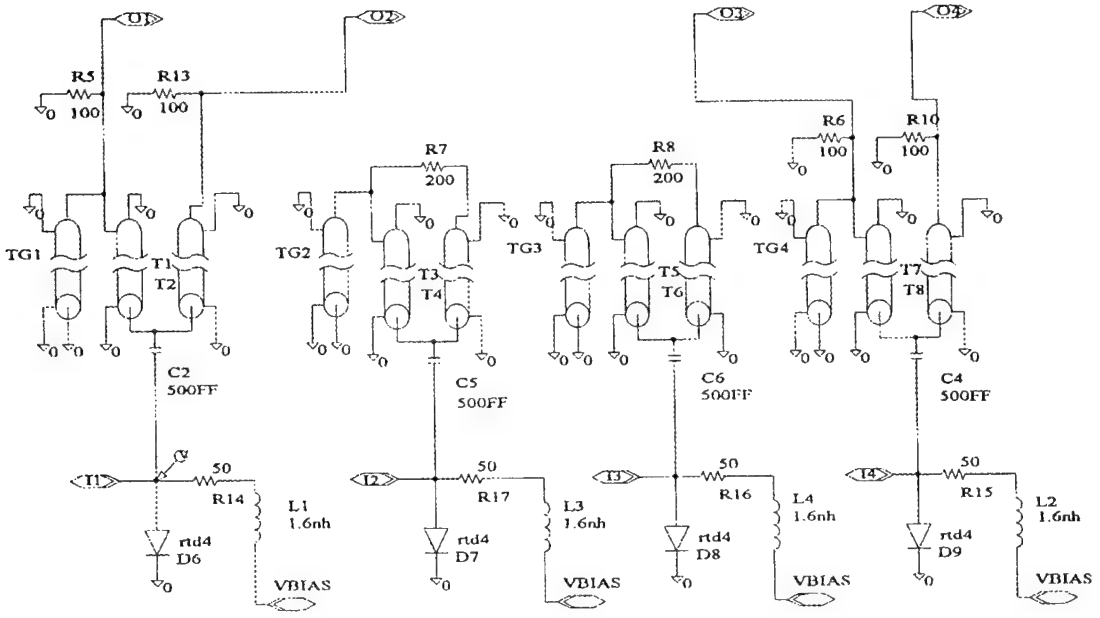

Figure 15: Single RTD driver / transformer array. Center two driver / transformers are not wired out to simplify the schematic and are included just to provide the proper loading.

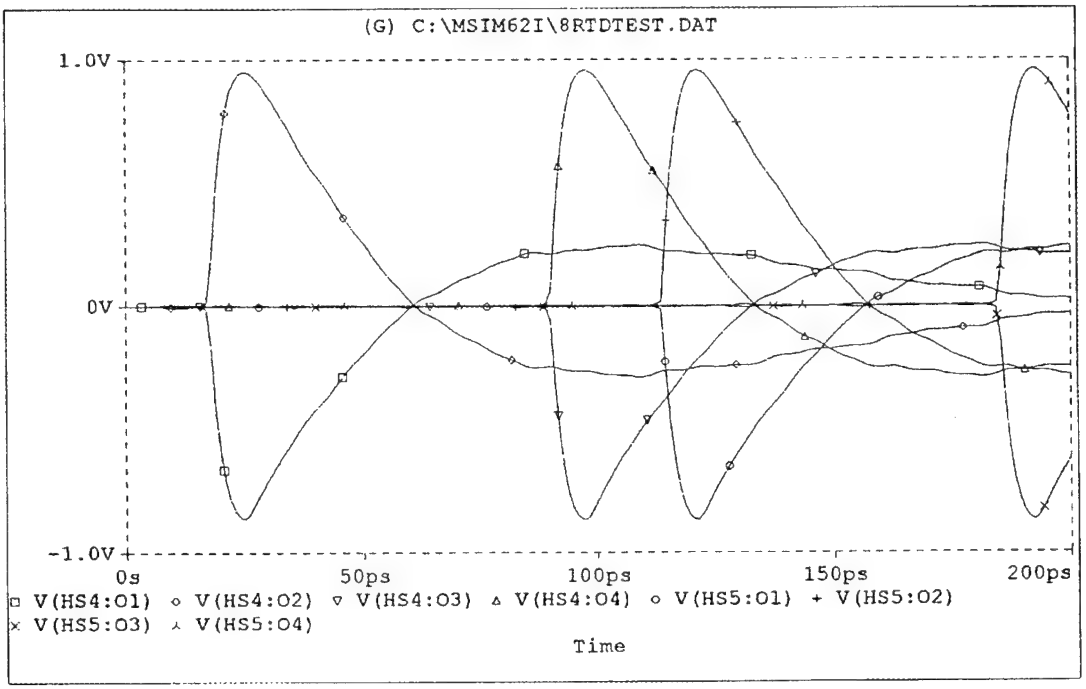

Figure 16: Operation of the RTD based digital time delay after triggering the array of RTD/ transformer drivers shown in Figure 15.

Timing Accuracy of RTD Circuits

It is clear that the RTD device has some key advantages as a high speed element as mentioned above. For low-cost high-speed instruments, the key advantage is that it switches extremely fast compared to devices with similar lithographic requirements and growth complexity. Because the RTD exhibits hysteresis when loaded with a resistance greater than its average negative differential resistance, it is a natural decision or timing element. The RTD has indeed been shown to be an excellent device for mm-wave triggering applications[1]. What remains to be determined is how well the RTD device performs in timing applications other than mm-wave triggering.

Basic RTD switch

There are two fundamental limitations to trigger circuit timing accuracy in general. The first is the fact that as the input signal approaches the decision threshold, the probability of random noise at the input or in the threshold level causing the signal to cross the threshold increases. The second is that the rate of rise of the input signal can affect the circuit time-delay.

Noise induced triggering is essentially the same problem as noise induced error in a digital communication system with the added complication of hysteresis in the threshold device. The presence of hysteresis means that the entire history of the waveform enters into the probability that the device will switch at a given moment, a stochastic process. The probability of a trigger at time t is equal to $P_1 p(n > x)$ where n is the random noise variable and x is threshold voltage minus $V_{in}(t)$. P_1 is the probability that the voltage will make it to $V_{in}(t)$ without resulting in a trigger. $p(n>x)$ is the probability that the noise will be sufficient to cross the threshold. P_1 is essentially unity up to $V_{in}(t)$ equal to the threshold voltage at which point it drops precipitously. The effect of P_1 is to reduce the timing uncertainty on the trailing edge of the distribution $p(n>x)$ particularly in the extreme edge where it is highly unlikely that the noise will remain sufficiently negative long enough for x get that far. Therefore, timing calculations based on $p(n>x)$ alone will tend to slightly overestimate the rms uncertainty.

Ignoring P1 described above, the trigger timing cumulative distribution function is given by: $p(n > x) = Q(x / \sqrt{\sigma_t^2 + \sigma_s^2})$. The probability density function in time is the just the time derivative of the cumulative distribution which is equal to the amplitude probability density of the input and threshold noise multiplied by the slope of the input waveform. For $V_{in}(t) = mt$, one standard deviation in time is equal to the amplitude noise standard deviation divided by the slope of the input waveform: $\sigma_{time} = \sqrt{\sigma_t^2 + \sigma_s^2} / m$. From this relation it is now possible to get a good estimate of the timing uncertainty based on input and threshold noise and it is obvious that the higher the signal slope the less uncertainty there will be for a fixed amount of amplitude noise.

The second limitation is the time delay associated with charging the RTD capacitance up to the point where the regenerative switching process takes control away from the input signal. This delay is governed only by the slew rate of the input signal and therefore will

vary directly with input slew rate variations. This effect is well known and is referred to as "slewing". Numerical simulation is required to get an accurate prediction for slewing effect on a circuit, but the trend can understood from the following analysis. Given that the input current increases linearly with slope *m*, the current available for charging the diode capacitance will also increase linearly as the I-V curve flattens out near the peak. The resulting time delay for a given voltage change ΔV is then $\Delta t = \sqrt{2C\Delta V / m}$. Thus the effect of slewing is minimized by reducing the device capacitance and making the peak in the I-V curve as sharp as possible to minimize the voltage change necessary to initiate the regenerative process.

Peak current density does not directly affect timing accuracy of the RTD switch in the above analysis because of the assumption that the ac signal current is significantly less than the peak current. If the ac signal current is comparable in magnitude to the peak current density, then the slewing affect must be considered throughout the RTD switching waveform and at some input current level, the output waveform becomes totally dominated by the input waveform with little sign of the RTD switching. Nevertheless, the only explicit dependence is on m, C, and ΔV. This suggests that, at least for single diode threshold detectors operating on isolated pulses, the diode capacitance and voltage are more important than the peak current density.

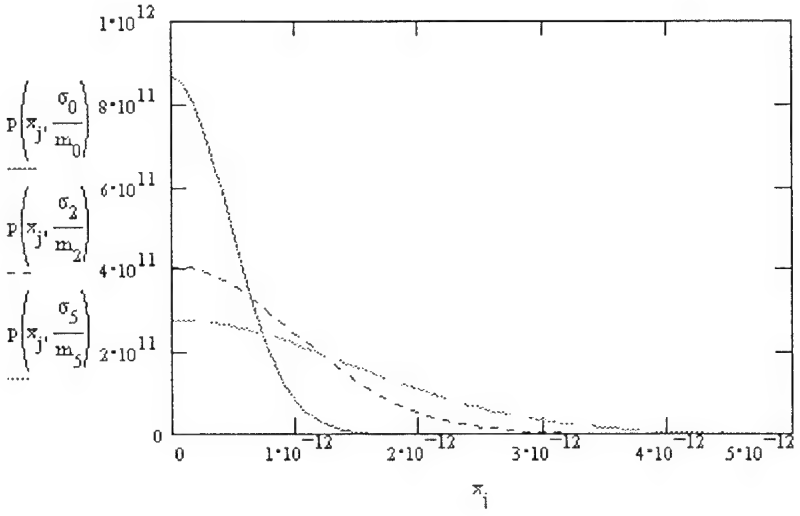

Figure 17: Timing histograms for case where bandwidth and slew-rate is fixed to a low value and area is increased. The smallest area device has the lowest sigma because shot-noise dominates (peak current increases with area but signal level held constant).

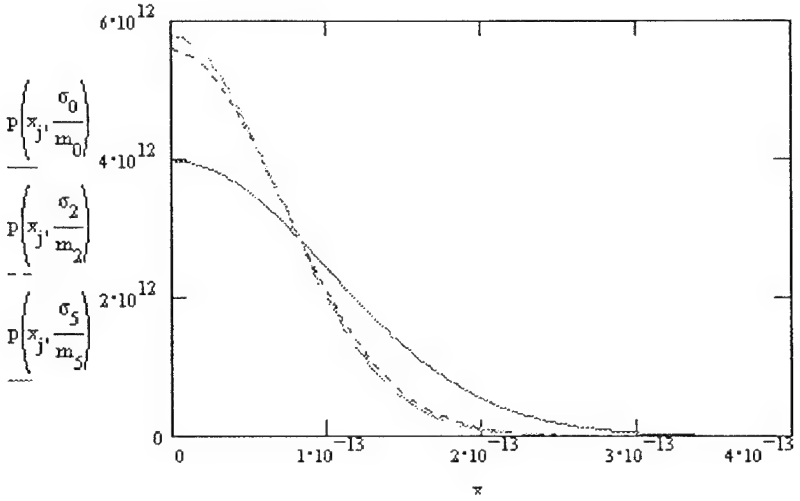

Figure 18: Timing histograms for the case where bandwidth and slew rate are determined by RTD device parameters. The larger devices perform better because thermal noise dominates.

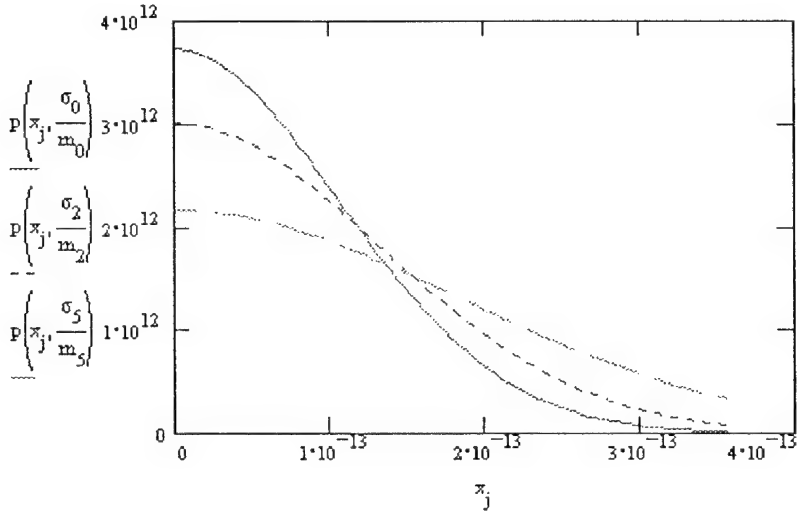

Figure 19: Timing histograms for the case where bandwidth and capacitance are limited by device parameters with the distribution resulting from "slewing" convolved in. A value of 5% was chosen for the slew-rate deviation to provide a case where it dominates.

The complete trigger circuit

Now that the basic limitations of the RTD trigger have been examined, the analysis can be extended to complete trigger circuit designs by use of circuit simulations. Here jitter and noise are simulated using parametric and "Monte Carlo" analysis. In parametric analysis, one or two parameters are varied systematically and the circuit response is studied. In Monte Carlo analysis, numerous parameters are varied randomly and the overall effect is examined with histograms of important parameters. Two circuits were chosen for this study. The first is a four diode sampling bridge as in Figure 4 driven by a ganged driver as in Figure 9. The second has the same driver, but the sampling bridge has six diodes.

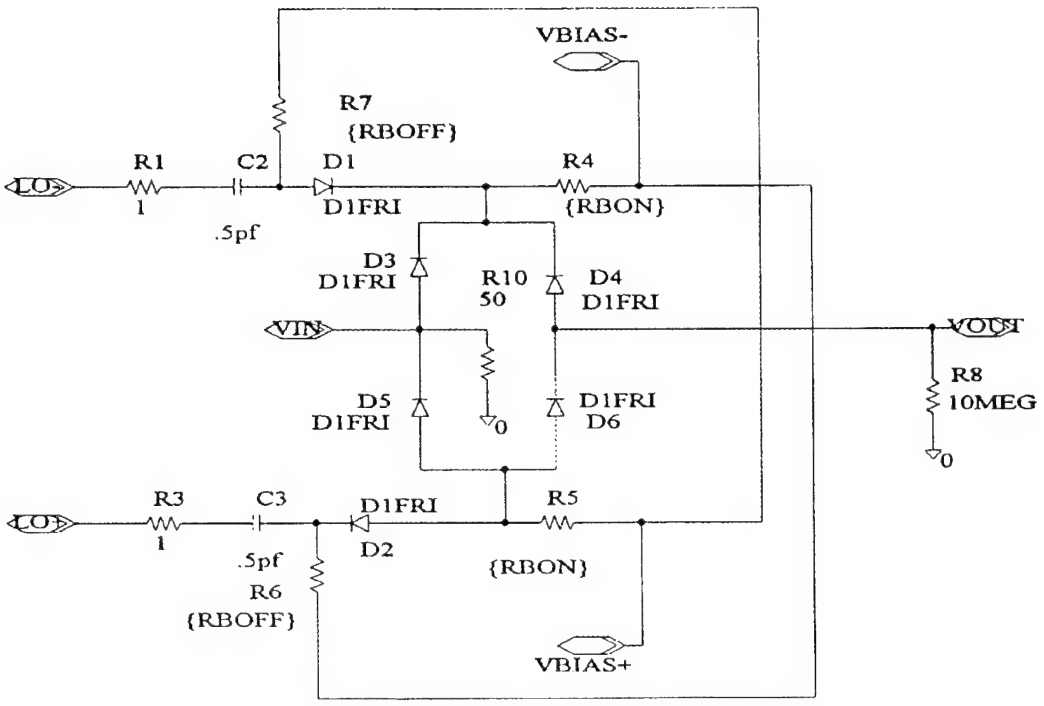

Figure 20: Six diode sampling bridge

The six-diode sampling bridge[9] shown in Figure 20 achieves isolation between the LO driver and the sampled input and output with diodes D1 and D2. These diodes are normally on and provide the off-state bias for the four diode bridge in the center. A sample is taken by turning D1 and D2 off allowing the bias supply to turn on the bridge through R4 and R5. Because D1 and D2 are off during a sampling instant, fluctuations in LO drive amplitude and symmetry have a reduced effect on the sample amplitude and offset.

The results of the parametric analysis are listed in Table 2. The efficiency is the change in sampled output voltage divided by the change in signal voltage measured in the linear portion of the characteristic. Max signal is the input signal voltage that causes the bridge to saturate. ΔV_0 is the change in output offset with fractional change in RTD bias. $\Delta t/t_r$ is the change in measured time interval with fractional change in RTD bias normalized to the trigger input rise-time. The 6-diode bridge uses the LO voltage slightly less efficiently producing less sample efficiency and a lower maximum signal. However, the 6-diode bridge has less than half the offset voltage sensitivity to RTD bias change. This is a measure of the isolation achieved by the additional diodes. The timing error in both cases is dominated by the change in threshold level at the trigger input RTD and has little to do with the sampling bridge itself. Clearly, the trigger input RTD must have exceptionally stable bias if longer rise-time signals are to provide accurate timing.

Table 2: Efficiency and sensitivity to fractional change in RTD bias

Parameter	4-diode bridge	6-diode bridge
efficiency	.41	.39
Max signal (V)	.8	.7
ΔVo (V)	.11	.05
$\Delta t/t_r$	4.44	4.74

These results can now be applied to the specific application of time-interval measurement. Beyond the obvious error that is induced by trigger threshold fluctuation, the most important error term is the output offset change with RTD bias. The RTD bias can change as a result of changing temperature, cross-talk from nearby circuitry, noise on the bias line, or device instabilities. The combined effect of these sources on RTD bias must be kept less than the value dictated by the sensitivity of Table 2 and the necessary signal to noise ratio. The signal level available is dependent on the application. Table 3 lists a few applications and their required bias stability. It is assumed that time is being measured with a 6-diode sampling bridge sampling the voltage of an interpolation function with a slope of 10^9 V/s. Δt is the required time resolution and $\Delta I_b/I_b$ is the required bias stability determined by the either offset, or trigger considerations.

Table 3: Summary of RTD stability requirements for target applications

Application	Signal rise-time	$\Delta\tau$	$\Delta I_b/I_b$	Limitation
Optical signal	100 ps	1 ps	0.2%	trigger
MCP pulse	50 ps	1 ps	0.4%	trigger
mm-wave	5 ps	0.1 ps	0.08%	offset

The first application in Table 3 is timing measurement of optical signals as required for timing verification in optical networks. The second, "MCP pulse" refers to timing measurements of pulses from a micro-channel plate. These devices are used to intensify electron signals from photocathodes or atomic particles striking the MCP directly. This application includes most physics experiments including time-of-flight mass spectroscopy and fluorescence spectroscopy. The last application is mm-wave signal timing to directly extract the mm-wave signal phase. In this case, the signal slew rate is so high that the trigger does not limit the timing accuracy. Here it is the error in measuring the interpolation function due to offset fluctuations that limits timing accuracy.

Photonic Switching

Since many of the applications for high-speed measurement involve optical signals, it is very desirable to switch the RTD optically. The tunneling layers themselves are too thin to be useful absorbers, the emitter too heavily doped, and the collector on the wrong side of the device to contribute to electron tunneling. The only practical approach is to add a layer on top of the RTD emitter to act as the absorbing layer. This approach is discussed in the section entitled "Process Compatibility of RTDs and Schottky Diodes."

Photonic switching using the additional absorbing layer with an additional P-type contact layer to form a PIN diode has been demonstrated by S.C. Kan, et. al.[10] The significance of this work is the flexibility in biasing the RTD and the photodiode, the quality of the photodiode, and the switching result. A representation of their approach is shown in Figure 21. Since the RTD can be resistively biased near the peak current and the photodiode signal merely initiates the switching action, the switching performance is the same as when triggered by the Thevinin equivalent voltage source. For a device biased with a 50 ohm resistor and connected to a 50 ohm load and assuming 1mA of photocurrent, the equivalent voltage source is 25 mV. This is too small to achieve reliable switching.

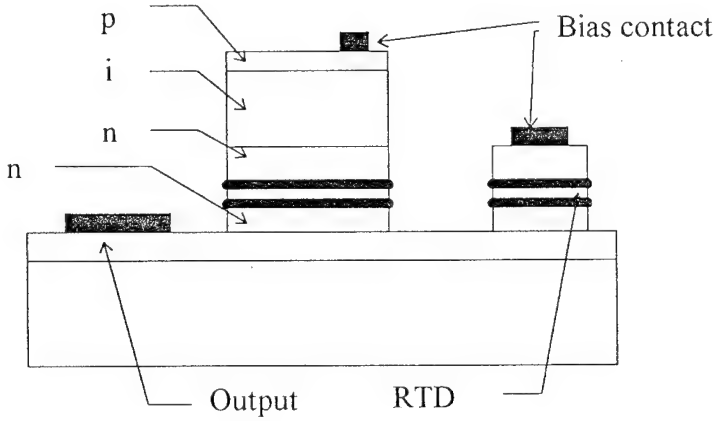

Figure 21: Representation of approach described in reference 10.

To achieve voltages on the same order as the peak voltage of the RTD, it is necessary to scale the resistors up and the device areas down to preserve speed and proper switching. In the referenced paper, the RTD design was also modified to work at very low peak-current density and high impedance levels. For high-speed operation, the current density must be maintained as high as possible. The trade-off involved can be expressed mathematically as:

1. $R_{eq} > 2R_n$
2. $R_n = (V_v - V_p)/(J_p - J_v)A_{RTD}$
3. $V_{eq} > V_p/3$
4. $V_{eq} = I_{pd}R_{eq}$
5. $C_L < \tau/R_{eq}$
6. $C_L = C'_{pd}A_{pd} + C'_{RTD}A_{RTD}$

The first equation assures bistability, the second defines the average negative resistance used in (1), the third assures reliable triggering, the fourth defines the equivalent voltage used in (3), the fifth limits the load capacitance for a given required time constant, and the sixth defines the load capacitance in terms of the photodiode and RTD capacitance per unit area. From (5) and (6) it is clear that minimum R_{eq} maximizes photodiode area. The minimum value of R_{eq} will be determined by either (1) or (4) depending on the available photocurrent. Both areas are maximized if (1) and (4) are just satisfied. The area is then found from (5) and (6):

$$A_{pd} < \tau I_{pd}/V_{eq}C'_{pd} - 2[C'_{RTD}/C'_{pd}][(V_v - V_p)/V_{eq}][I_{pd}/(J_p - J_v)]$$

Typical values for the remaining parameters are: I_{pd}=1mA, V_{eq}=.3V, $C'_{pd}=10^{-7}$ F/cm^2, $C'_{RTD}=C'_{pd}$, $V_v - V_p = V_{eq}$, and $J_p=2\text{x}10^5$A/cm^2. For τ=1 ps, the required area is about 3 μm^2 for the photodiode and 1 μm^2 for the RTD with an equivalent load resistance of 300 ohms. Clearly, picosecond photonic switching with RTDs is a big challenge with this structure unless substantially more than 1mW of optical power is available.

The MSM photodiode has different scaling rules and is therefore a possible solution to the scaling problem, but demands deep sub-micron lithography to achieve picosecond speeds. Evidently, moderate power photonic switching of RTDs is limited to the ~10ps and above speed regime for practical device areas and low-cost manufacture. In this speed range, the importance of integrating the photodiode is not as great, but could still be significant for array applications.

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Appendix A: Subcontractor's Final Report

Chapter 1: Introduction

1.1 General Description:

Since the seminal work of Tsu and Esaki in 1973 [1], a great amount of effort has been spent on improving the characteristics of Double-Barrier Resonant Tunneling Diodes (DB-RTD's). Currently, RTD's are the widest bandwidth semiconductor devices with gain which have been used to build microwave oscillators with oscillation frequency in the range of 400-700 GHz [2,3], trigger circuits operating up to 110 GHz [4,5], and a wide range of high speed logic or switching circuits [6-8].

For practical applications, GaAs-based RTD's are favored over GaSb- and InP-based structures due to the maturity of material growth and processing techniques. Also, for integration purposes, use of a GaAs-based structure enables us to take full advantage of the previous work on high-speed sampling circuits and photodiodes [9-11].

The structure is grown by Metal Organic Chemical Vapor Deposition (MOCVD) technique, which has received a great amount of attention as a source of high-quality low-cost material with the capability of growing phosphorous-based and quaternary compositions.

Table 1.1 summarizes the DC electrical characteristics determined by the circuit requirements.

Characteristics:	Value:
Voltage Swing	>2 volts
Peak Current Density (PCD)	100 to 200 kA/ cm^2
Peak Current	10 to 20 mA
Peak Voltage	1 Volt
Peak to valley ratio (PVR)	>3
Rise-time	<2 ps

Table 1.1 RTD's electrical characteristics determined by circuit requirements.

1.2 Report Structure

In chapter 2 we describe the code developed to model the electrical performance of RTD's.

Chapter 3 includes a study of the effects of composition and thickness of different layers on electrical characteristics of RTD's, using the developed simulation program. This chapter is basically aimed to provide us with an optimized structure to exceed (or meet) the electrical characteristics listed in Table 1.1.

The fabrication process sequence for the suggested structure is discussed in detail in chapter 4. Finally, chapter 5 displays the results of our measurements for the fabricated devices, and includes the pertinent discussions.

1.3 Accomplishments:

As a result of this work we succeeded to design and fabricate RTD's with more than 2 times higher peak current densities (PCD's) than the ones reported for GaAs-based

RTD's [12] and more than 3 times higher PCD values than those obtained for any type of MOCVD-grown RTD's [13]. Also, we introduced and verified the concept of using the second resonant energy level in a strained-layer quantum-well RTD as the working (tunneling) level, which results in very high PCD values, and, in general, could be applied to any type of RTD. The results will be presented at the EDS' Device Research Conference in June 1996. A copy of the conference abstract is enclosed as Appendix A.

Chapter 2: Device Simulation

The most common method to calculate the resonant tunneling current in a multi-barrier structure is to use the global transmission coefficient for a coherent wavefunction throughout the heterostructure [1,14]. The transfer matrix method can be used to calculate the transmission coefficient for such a structure. Together with the Fermi distribution of electrons behind the structure, the tunnel current is calculated by integrating over the transverse direction. The numerical method used to carry out the above procedure is based on the algorithm suggested in ref. [15]. The whole code is written in MATLAB.

2.1 Calculation Procedure:

A) Transmission Probability across Arbitrary Potential Barriers

In the transfer matrix method , instead of dealing with continuous variations of potential energy, we divide the potential barriers into segments, such that the potential can be regarded as a constant. By reducing the size of our divisions a good approximation of the

potential distribution can be achieved. If we assume that our structure is divided into N segments, the potential, $U(x)$, the effective, $m^*(x)$, and permittivity, $\varepsilon(x)$, for every segment can be defined as follows:

$$\begin{aligned} U_j &= U[(x_{j-1} + x_j)/2], \\ m^*_j &= m^*[(x_{j-1} + x_j)/2], \\ \varepsilon_j &= \varepsilon[(x_{j-1} + x_j)/2]. \end{aligned} \tag{1}$$

For the wavefunction ψ_j in the jth region, associated with an electron with energy E moving perpendicular to the interfaces, one can assume:

$$\psi_j = A_j \exp(ik_j x) + B_j(-ik_j x), \tag{2}$$

where

$$k_j = \sqrt{[2m_j^*(E - U_j)]}/\eta \tag{3}$$

Due to the continuity of $\psi_j(x)$ and $1/(m^*_j)(d\psi_j/dx)$ at each boundary, the coefficients A_j and B_j in the Eqn. 2 can calculated from:

$$\begin{pmatrix} A_j \\ B_j \end{pmatrix} = \prod_{l=0}^{j-1} M_l \begin{pmatrix} A_0 \\ B_0 \end{pmatrix}, \tag{4}$$

where

$$M_l = \frac{1}{2}\begin{bmatrix} (1+S_l)\exp[-i(k_{l+1} - k_l)x_l] & (1-S_l)\exp[-i(k_{l+1} + k_l)x_l] \\ (1-S_l)\exp[i(k_{l+1} + k_l)x_l] & (1+S_l)\exp[i(k_{l+1} - k_l)x_l] \end{bmatrix} \tag{5}$$

and

$$S_l = \frac{m^*_{l+1}}{m^*_l}\frac{k_l}{k_{l+1}}. \tag{6}$$

Since $A_0=1$ and $B_{N+1}=0$ in eqn. 4, we can calculate the transmission amplitude A_{N+1} as

$$A_{N+1} = \frac{m^*_{N+1}}{m^*_0}\frac{k_0}{k_{N+1}}\frac{1}{M_{22}}, \tag{7}$$

where

$$M = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} = \prod_{l=0}^{N} M_l. \tag{8}$$

B) Transmission-Current Calculation:

The total applied voltage V can be decomposed into 3 components, $V=V_a+V_b+V_d$, where V_a, V_b, and V_d are the voltage drops across the accumulation layer, the structure, and the depletion region, respectively. These values and the space charge n_s per unit area in the depletion layer are determined by solving the following equations simultaneously for a given value of V:

$$\exp(qV_a / kT) - qV_a / kT - 1 = q^2 n_s^2 / 2\varepsilon_0 kTN_D,$$

$$V_b = \int_0^{L_b} [qn_s / \varepsilon(x)]dx, \tag{9}$$

$$V_d = qn_s^2 / 2\varepsilon_{N+1} N_d$$

where N_d is the donor concentration in the semiconductor (assumed to be the same at both sides) and L_b is the thickness of whole structure. The Boltzmann's distribution is assumed to be an acceptable description of electrons distribution behind the structure in order to derive eqn. 10.

Having the potential distribution across the structure, the total current is:

$$I = \int N(E_x)T(E_x)dE_x,$$

$$N(E_x) = \left(\frac{4\pi m^* qkT}{h^3}\right) \ln\left(\frac{1+\exp\{[E_f(T)+V_a-E_x]/kT\}}{1+\exp\{[E_f(T)+V_a-V-E_x]/kT\}}\right), \quad (10)$$

where E_x is the electron energy associated with the motion normal to the interfaces, $E_f(T)$ is the Fermi energy, m^* is the effective mass of electron in GaAs, and $T(E_x)$ is the electron transmissivity factor (transmission probability) through the structure calculated in eqn. as A_{N+1}.

2.2 Example:

In order to check the accuracy of our modeling, the program was run for a structure with measured *I-V* curve [4]. Figures 2.1-a and 2.1-b show the structure and the corresponding measured *I-V* curve, respectively. Figures 2.2 and 2.3 are the calculated electron transmissivity and transmission current for the structure, respectively. Compared to the experimental results:

1- the peak current densities are basically the same,

2- the calculated peak voltage (1.1 volts) is slightly less than the measured one (1.4 volts) due to the voltage drop across the contacts, a parameter not included in our model,

3- the calculated valley current is much less than the measured one because our model only takes care of the transmission current caused by tunneling through the structure; however, the valley current is basically a consequence of various scattering processes such as optical-phonon scattering and interface-roughness scattering [16].

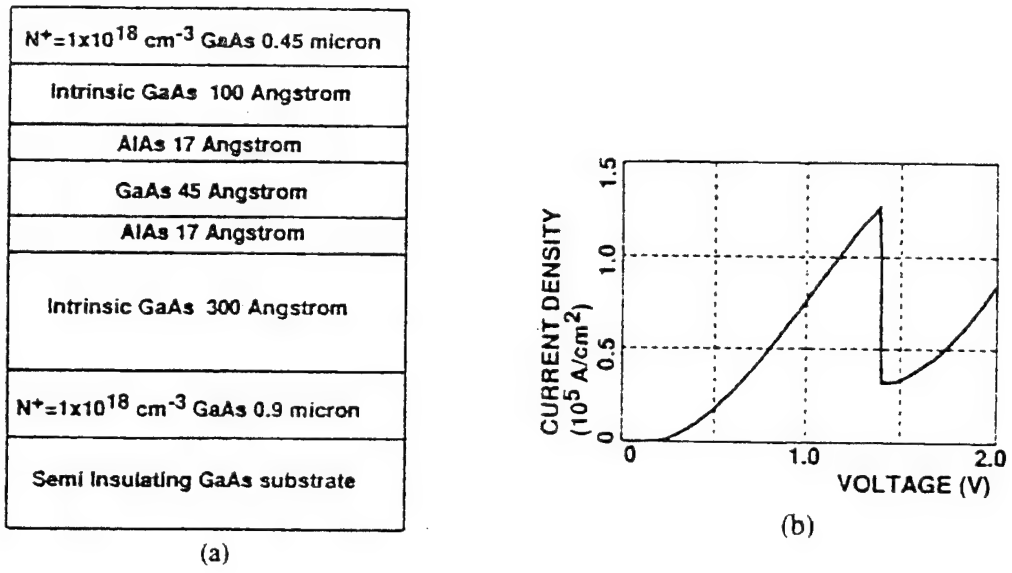


Fig. 2.1. a) Schematic of the epilayer design for RTD structure. b) Current density versus voltage characteristic of the RTD structure.

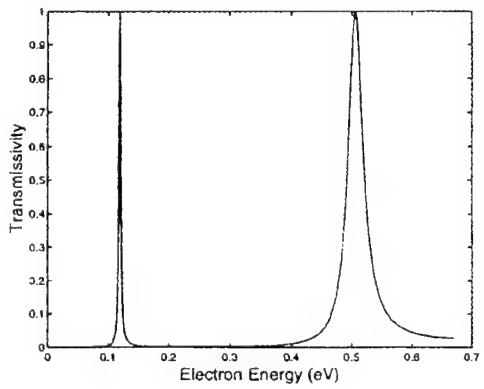


Fig. 2.2. Electron transmissivity as a function of energy for the structure shown in fig. 2.1-a.

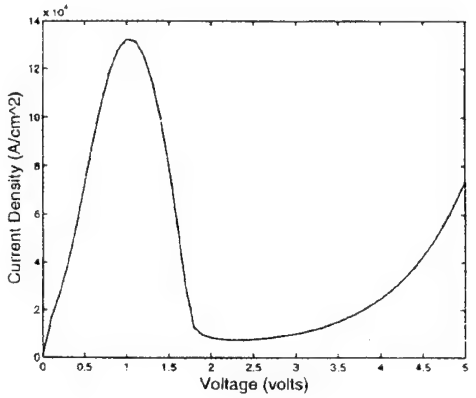


Fig. 2.3. I-V characteristic calculated for the RTD structure shown in fig. 2.1-a.

Chapter 3: Design Considerations

Using the simulation program explained in previous chapter, the effects of various material structures and geometrical parameters on the I-V curve of a DB-RTD are studied. This study includes the following aspects:

- The effects of barriers' width on the peak current density and peak voltage.

- A comparison between resonant tunneling through the first and second resonant energy levels.

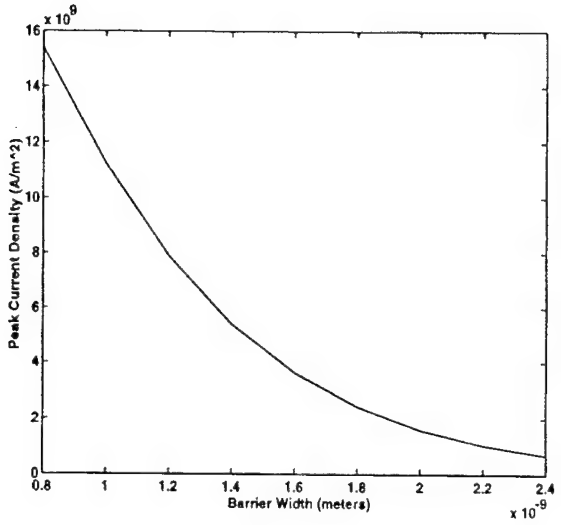
-The effect of well width on electrical characteristics of a RTD and the critical thickness for the well.

-Choice of material in a way to satisfy the above considerations.

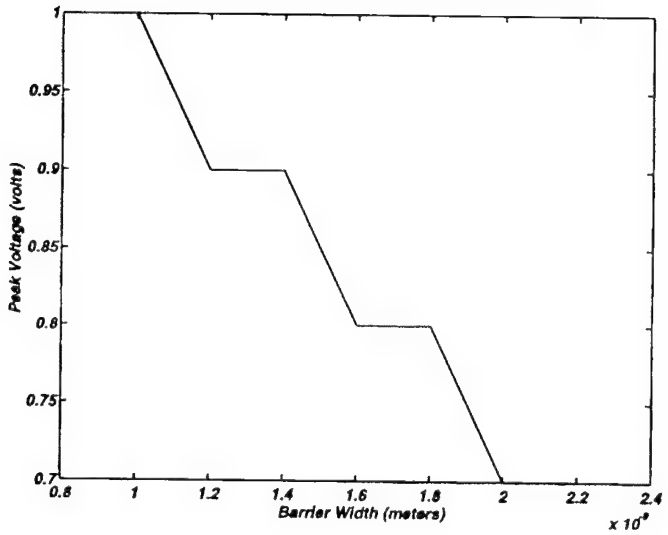
-Suggestions for optimizing the structure.

3.1 Barriers' width:

The effect of barriers width on peak current density has been extensively studied by various groups. Results of theoretical studies show that the peak current density in symmetric RTD structures decreases exponentially with increasing the thickness of barriers [17]. This result is supported by the experimental measurements [17,18]. Figures 3.1-a and b show results of our simulations for peak current density and peak voltage as a function of barriers width, respectively. Fig. 3.1-a shows that the peak current density decays exponentially as the barrier width increases. Fig. 3.1-b shows that the peak voltage slightly decreases with the barriers thickness which happens basically due to the better confinement of energy levels in the quantum well.



(a)



(b)

Fig. 3.1. a) Peak current density for a GaAs/$(In0_{.33}Ga_{0.67})_{0.5}In_{0.5}P$ structure as a function of barriers thickness (well width = 44 Å), b) peak voltage versus barriers thickness for the same structure.

Moving toward thinner barriers in favor of higher peak current densities is practically limited to a minimum of 4 monolayers (1 ML~2.8 Å). Structures with barriers thinner than ~12 Å are totally instable and associated with a very poor peak-to-valley ratio [18].

For our structure we suggest barriers as thin as 16 Å, which, according to previous work by Prof. Botez's group, is attainable by MOCVD growth in an Aixtron A-200 reactor.

3.2 Comparison between resonant tunneling through the first and second resonant energy levels:

The initial measurements done by the T. P. E. Broekaert et al. (ref. [19]) show that in an $In_{0.53}Ga_{0.47}As$/AlAs/InAs structure grown on InP substrate the peak current density for the resonant tunneling through the second energy level is almost 10 times greater than the peak current density associated with the first energy level for the same structure, fig. 3.2. This can be easily explained due to the fact that the second energy level is close to the top of the quantum well, and hence it is not as confined as the first energy level in the quantum well. In other words, by looking back at the plot describing the transmission probability of electrons versus energy in section 2.2, (fig. 2.2), it can be easily seen that the transmission spike corresponding to second level is much wider (i.e. less confined) than the one for the first level; which means that electrons over a wider range of energy have the chance to tunnel through the structure at the same time. Since the resonant tunneling current is the sum of transmission probability ,T(Ex), times the electron distribution, N(Ex), over the whole range of energies above the conduction band (eqn. 10), it is expected from the transmission probability plot, that the tunneling current for the second energy level will be much higher than the one through the first level.

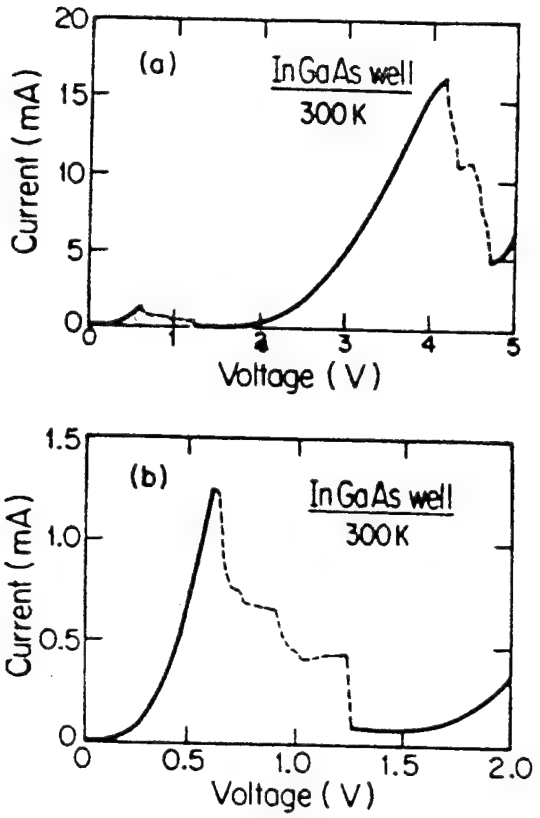


Fig. 3.2. I-V characteristics of a 10×10 μm^2 pseudomorphic $In_{0.53}Ga_{0.47}As/AlAs$ RTB diode a) showing two resonances at room temperature, I_{p2}=17 ma, I_{p1}=13ma, and J_{p2}/J_{p1}=1, b) showing in more detail the first resonance (from ref. [19]).

However, the peak voltage for the second resonant level is so high (~4.1 volts) that it is impractical for any application. During our discussions we realized that if we make the quantum well deep enough to adjust the second level close to the bottom of the conduction band of the emitter (i.e. lowering the peak voltage into the useful range around 1 volt), one can achieve resonant transmission through the second level. However, it was unclear whether the transmission probability function will still keep its wide bell-like shape. Unexpectedly and fortunately, the answer to this question was positive.

Figure 3.3 is a comparison between two structures with similar barriers and well thicknesses. The first structure is a GaAs/AlAs RTD, and the second one is a

$In_{0.3}Ga_{0.7}As$/AlAs RTD, for which the bottom of the quantum well is ~0.2 eV lower than the bottom of the emitter conduction band (here GaAs); figures 3.3-a and b are pictorial descriptions of the band diagrams for those two structures. Figures 3.3-c and d show the electron transmissivity through the GaAs/AlAs and $In_{0.3}Ga_{0.7}As$/AlAs structures, respectively. It can be seen that the transmission probability for the second level in the deep-quantum-well structure is still broader than the one corresponding to the first level in GaAs/AlAs structure. Consequently, the peak current density for the deep-quantum-well RTD is almost 5 times higher than the one for GaAs/AlAs.

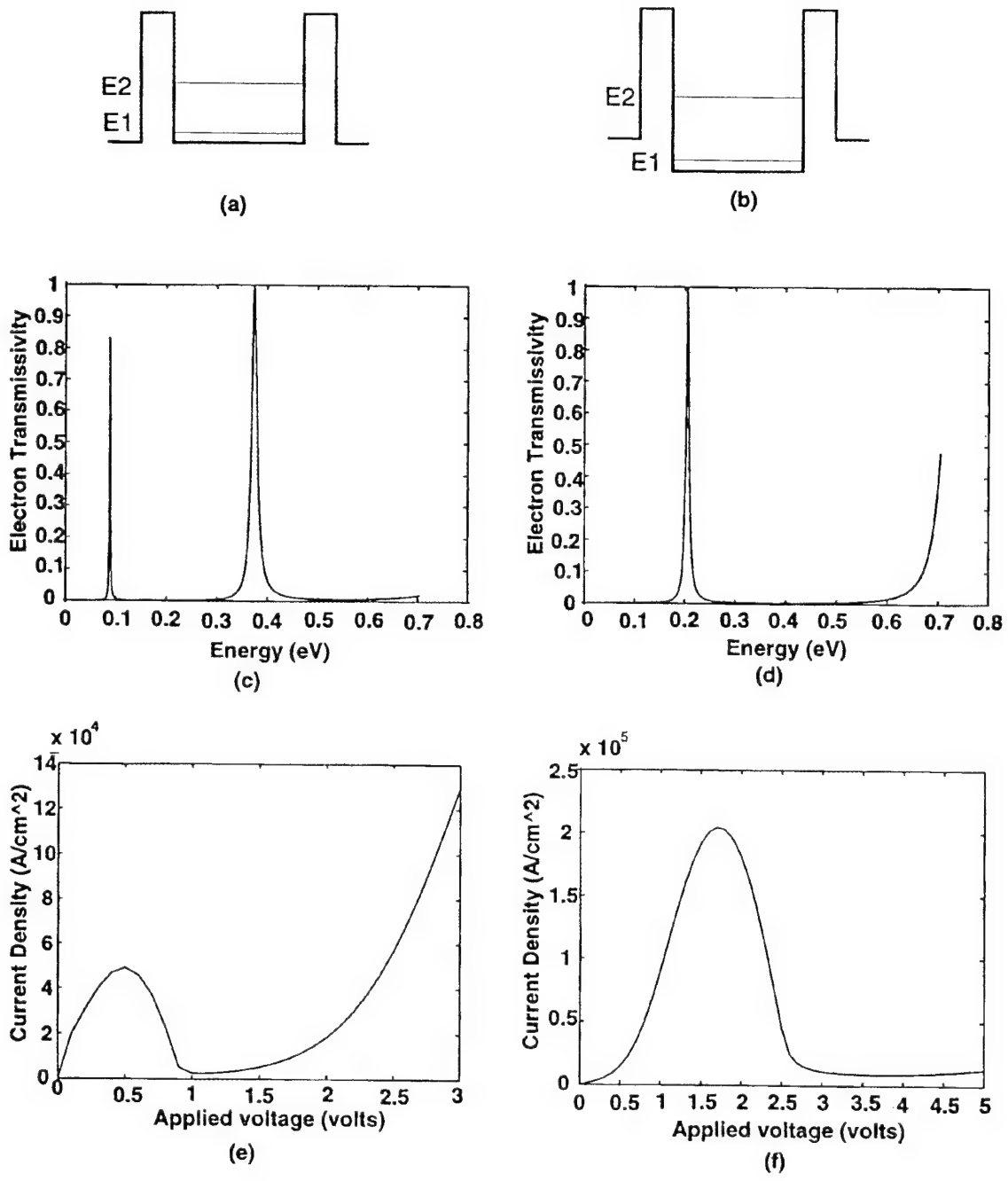


Fig. 3.3. A comparison between GaAs/AlAs and $In_{0.3}Ga_{0.7}As$/AlAs structures with the same barriers and well thicknesses. a,b) band diagrams, c,d) transmission probability as a function of energy, e,f) current density as a function of applied voltage.

3.3 The effects of well width and depth on peak current density and peak voltage:

Figure 3.4 shows that for a GaAs/$(In_{0.33}Ga_{0.67})_{0.5}In_{0.5}P$ structure the width of well has an effect on peak current density similar to the one of the thickness of barriers; i.e., the peak current density decreases almost exponentially with the thickness of the well.

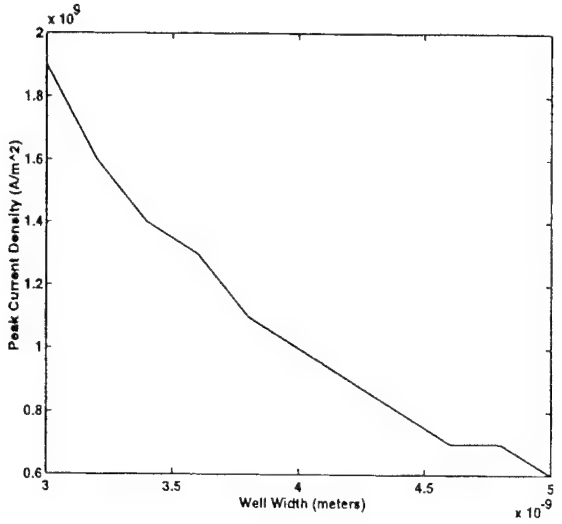


Fig. 3.4. Peak current density for a GaAs/$(In_{0.33}Ga_{0.67})_{0.5}In_{0.5}P$ structure as a function of well width (thickness of barriers=16 Å).

However, for a structure with a deep quantum well (e.g. $In_{0.3}Ga_{0.7}As$) this dependence is somewhat more complicated (see Fig. 3.5). The first peak in Fig. 3.5 corresponds to resonant tunneling through the first level; as we increase the well width, the first level falls below the bottom of conduction band of the emitter, and consequently the PCD value drastically decreases. By increasing the well width further the second level starts to get closer to the bottom of emitter conduction band, and thus a second transmission peak appears.

At the first look, it seems that in spite of our discussion in the preceding section, resonant tunneling trough the first level results in a greater peak current density than the second level. However, it is not the correct conclusion, because the maximum PCD for the first level happens at much narrower well widths (around 20 Å) than the maximum for the second level (almost 50 Å). Recalling the fact that the PCD decreases exponentially with well width (Fig. 3.4), it becomes clear that although the PCD for resonant tunneling through the second level in a 50Å-well RTD is greater than the one for tunneling through the first level in a similar structure, it might be lower than the PCD of tunneling through the first level in for a 20Å-well RTD.

However, Fig. 3.5 also shows that the sensitivity of PCDs associated with the resonant tunneling through the first level due to the variations of the well width is almost two times higher than the sensitivity of PCDs associated with the second level, i.e., any slight deviation in the well width during the growth process may drastically affect the PCD of the grown structures designed to tunnel through the first energy level. For this reason, in deep-quantum-well structures, resonant tunneling through the second energy level is advantageous over tunneling through the first level.

Figure 3.6 shows the peak voltage as a function of well width for the same $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ structure (barriers width=16 Å). There is a critical well width for each of the first and second energy levels, since beyond that width the corresponding resonant energy level falls below the bottom of emitter conduction band, it results in a sudden increase in the peak voltage. This critical width for the first and second energy levels is 30 and 72 Å, respectively. In our optimized structure the desired well width should be away from the critical width with a safety margin that depends on the

precision of our growth process. Typically, we chose a 10 Å safety margin for the structures we grew.

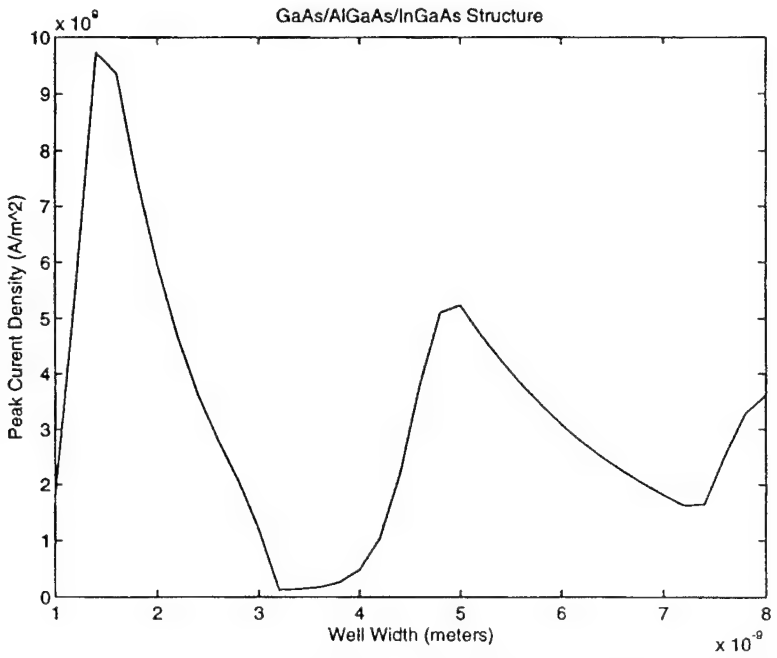


Fig. 3.5. Peak current density as a function of well width for a $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ structure (barriers width=16 Å).

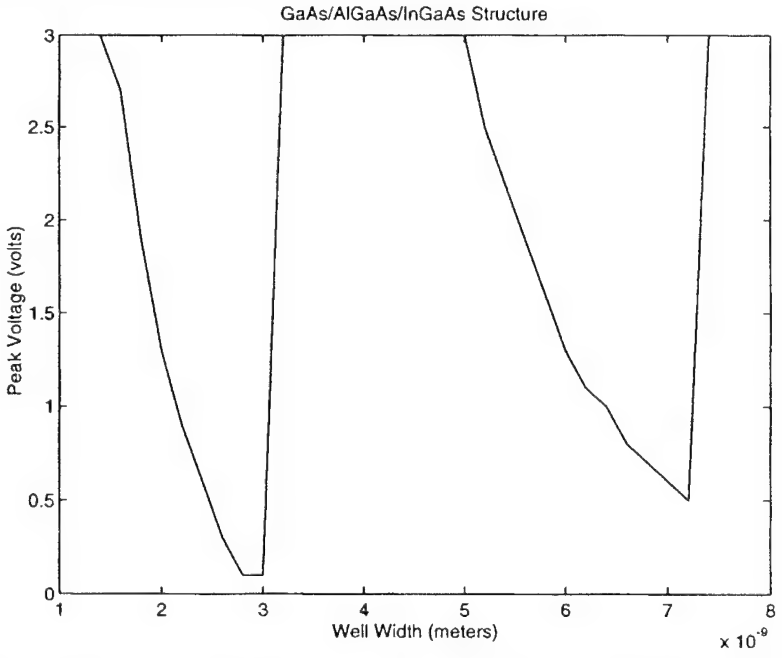


Fig. 3.6. Peak voltage as a function of well width for a $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ structure (barriers width=16 Å).

3.4 Optimized Structure:

Due to the fact that peak current density is the main figure of merit for high-speed RTD switching applications, and based on the results of our simulations in the preceding sections, the strained-layer $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ material system looks as the appropriate choice for high peak current densities at the level of 300-400 kA/cm^2.

PCD's at the level of 300 kA/cm^2 together with peak voltages as low as 1 volt can be obtained by two different schemes (Fig. 3.5):

1) Resonant tunneling through the first energy level in a structure with a narrow well (~20 Å).

2) Resonant tunneling through the second energy level in a structure with a wide well (~60 Å).

Due to a better tolerance with respect to the possible variations in the well width from the target value, and also, because of the novelty of the concept, we decided to invest our efforts on the implementation of RTD's operating on resonant tunneling through the second energy level.

Chapter 4: Fabrication Process

The fabrication process is consisted of two major steps:

1- structure growth, and

2- device fabrication.

In material growth, we basically concentrated on two different material structures: $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ and $(In_{0.33}Ga_{0.67})_{0.5}In_{0.5}P/\ In_{0.3}Ga_{0.7}As/GaAs$. The growth was carried out by Metal Organic Chemical Vapor Deposition (MOCVD) technique and the quality of the grown structures was examined by transmission electron microscopy (TEM). Also, by running TEM on several test structures, the growth rates for various layers were very well calibrated (at the level of a few Å). The device process basically consists of various steps to fabricate proper contacts for emitter and collector sides, and etching mesas to form isolated devices. Due to the crucial effect of series resistance on the negative differential resistance of RTD's, a two-step process was used to make a low-resistance ohmic contact on top of the mesa (emitter side). Metal contacts were deposited by e-beam metal deposition and patterned by the lift-off technique.

A total of three different masks was used throughout the fabrication process (Appendix B); the most precise alignment needed in the process being the alignment of $3\times3\ \mu m^2$ windows into an SiO_2 isolation layer with the $3\times3\ \mu m^2$ top metal contacts (that was easily achieved by using a Karl Suss MJB3 mask aligner). The complete fabrication process will be explained in greater detail in section 4.2.

4.1 Material Growth

The RTD structure is grown using low-pressure (50 mbar) metalorganic chemical vapor deposition (LP-MOCVD) in an Aixtron A-200 system, at a growth temperature of 700 ^{0}C. The metalorganic precursors are trimethylgallium, trimethylaluminum, and trimethylindium.The group V source is arsine with silane used as an n-type dopant. Prior to growth of the RTD structure, the solid composition (x) of $Al_xGa_{1-x}As$ was measured using x-ray diffraction, as a function of the aluminum gas-phase mole-fraction. Growth rates were obtained from film-thickness measurements using scanning electron microscopy. Similarly, the solid composition (y) of $In_yGa_{1-y}As$ was determined from x-ray diffraction rocking curve measurements on thick (relaxed) layers (Fig. 4.1). To improve the quantum-well interfacial morphology, RTD structures were grown on nominally exact (100) +/- 0.1^0 GaAs substrates [20]. The reason for selecting such a substrate orientation was that studies at UW-Madison of strained-layer InGaAs quantum-well structures, via atomic force microscopy (AFM) [20], indicate that growth using exact on-orientation substrates significantly improves the interfacial structure by eliminating step-bunching. After growth of the RTD structure, the layers thicknesses were confirmed using high-resolution TEM lattice imaging.

The results of TEMs showed that for the $(In_{0.33}Ga_{0.67})_{0.5}In_{0.5}P/In_{0.3}Ga_{0.7}As/GaAs$ material structure, the second barrier grown on top of the $In_{0.3}Ga_{0.7}As$ strained layer, due to the

low thickness and quaternary composition of the InGaInP, does not have uniform quality and contains a considerable amount of dislocations. Therefore, the $(In_{0.33}Ga_{0.67})_{0.5}In_{0.5}P/In_{0.3}Ga_{0.7}As/GaAs$ structure was ruled out as a material choice. By contrast, the TEMs of $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ structures showed a clear image of distinct layers with relatively abrupt transitions at interfaces. Fig. 4.2 shows the TEM for a $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$ structure grown with 16Å-thick barriers and 57Å-thick well. From a high-resolution TEM lattice image (Fig. 4.3), one can estimate the thicknesses of the first barrier (from the bottom), well, and second barrier as 14.5 Å, 57 Å, and 13 Å, respectively, which are in good agreement with the target values.

A schematic view of the grown structure is shown in Fig. 4.4 which includes (from bottom to top): a 300 Å spacer layer to reduce the intrinsic capacitance of the device, 14 Å $Al_{0.8}Ga_{0.2}As$ barrier, 57 Å $In_{0.3}Ga_{0.7}As$ well, the second barrier, and a 100 Å layer of intrinsic GaAs to separate the structure from the doped top layer.

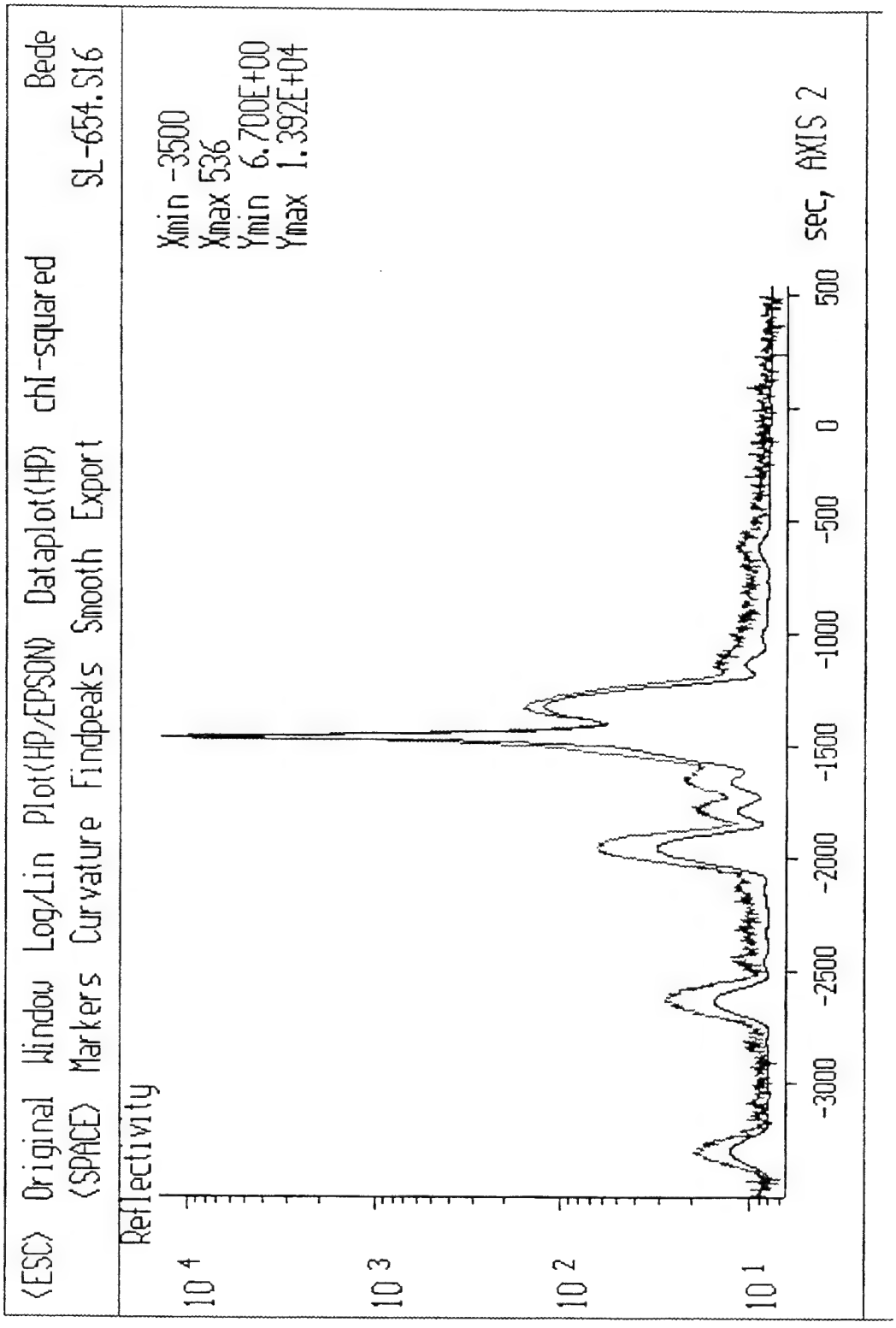


Fig. 4.1. Double crystal X-ray diffraction used to determine the solid composition of epi layers.

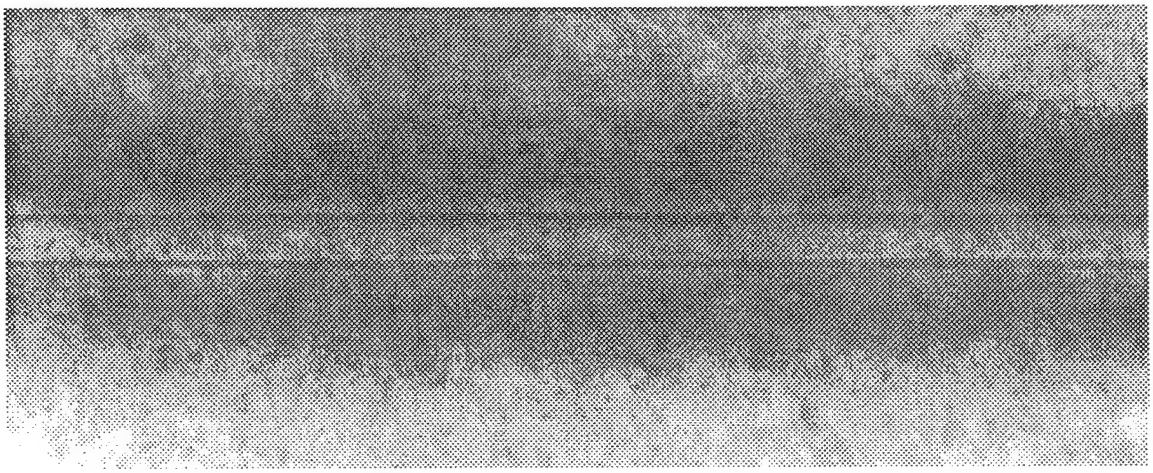


Fig. 4.2. TEM (002) dark field image showing the buried epi layer.

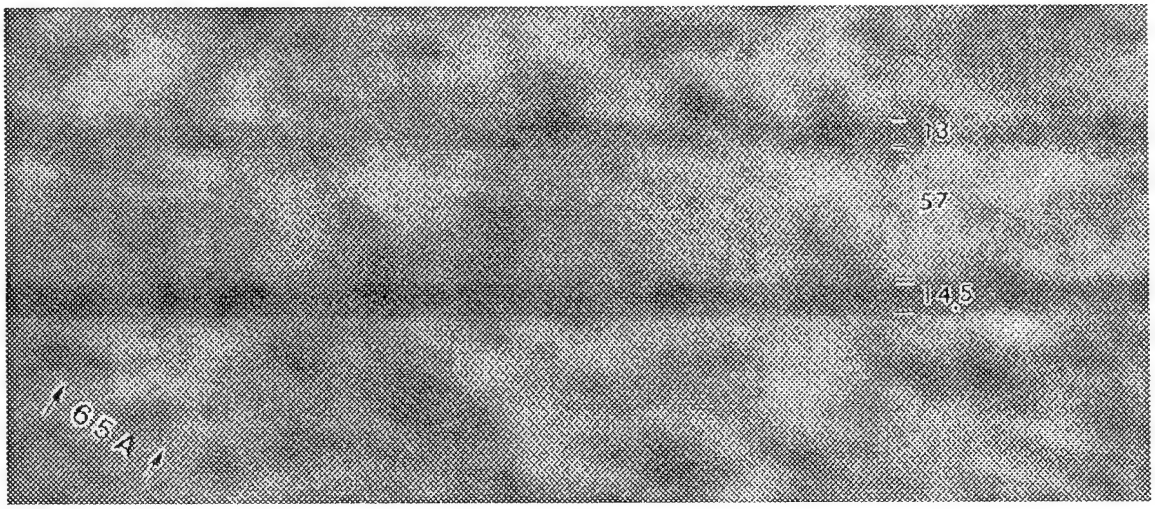


Fig. 4.3. High resolution TEM lattice image showing the layer morphology. The arrows show 20 (111) GaAs lattice spacings of 3.26 Å each. The total spacing between the arrows is 65 Å.

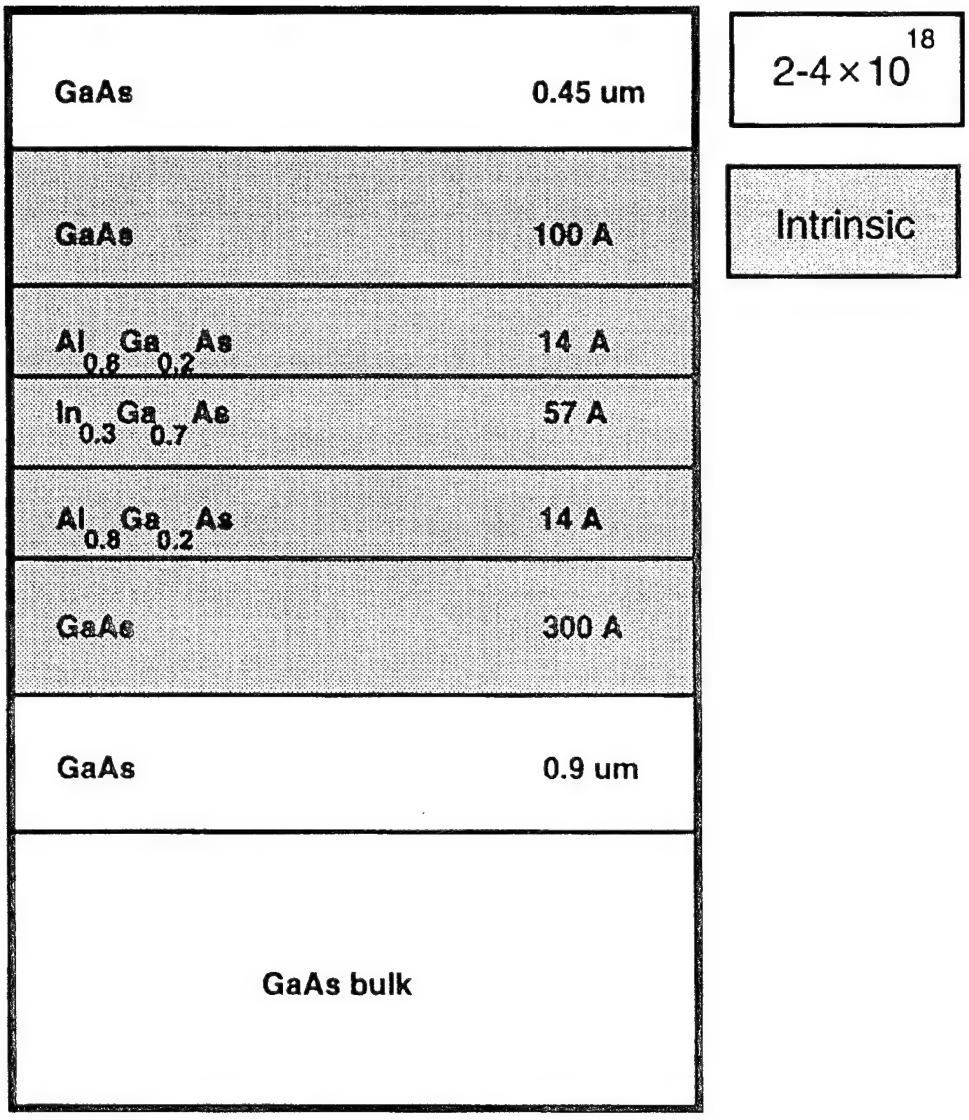


Fig. 4.4. Schematic view of the grown structure: $In_{0.3}Ga_{0.7}As/Al_{0.8}Ga_{0.2}As/GaAs$.

4.2 Device fabrication

The device fabrication starts with the deposition of the top metal contact using e-beam metal deposition. In order to make a good ohmic contact, we use a sequence of various metal layers like: Ge-Au/Ge-Ni-Au. The deposited metal is patterned to 3×3 μm^2 squares separated by 1 mm from each other. Then, using chemical etching, mesas of different sizes (from 5×5 μm^2 to 8×8 μm^2) are etched around contacts. After covering the whole wafer with 1000Å-thick SiO_2 film as an isolation layer, 3×3 μm^2 windows are opened on top of the buried contacts. Then, the second layer of metal, composed of Ti-Pt-Au layers, is deposited on the wafer. In order to facilitate cleaving the wafer into devices, the wafer is thinned to 150 μm by mechanical lapping. After depositing the back contact (Ge-Au/Ge-Ni-Au), the contacts are alloyed by rapid thermal annealing (RTA) in order not to damage the structure (at 400 °C for 30 seconds). The last step is to cleave the wafer into devices. Fig. 4.5 shows a cross-sectional view of the device. The major fabrication steps are listed in Table 4.1.

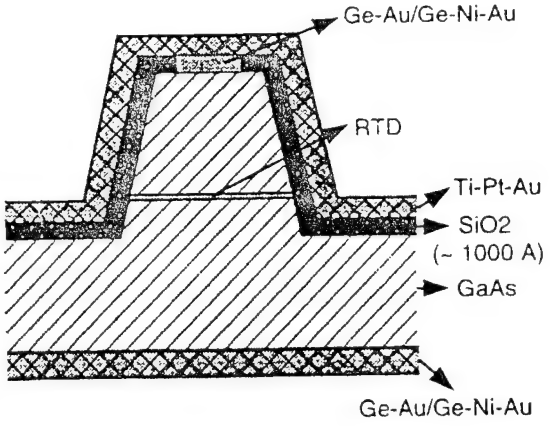


Fig. 4.5. A cross-sectional view of the fabricated device.

Major fabrication process steps:	Details
A) MOCVD Growth:	1-System Calibration. 2-Wafer preparation (if necessary). 3-MOCVD device growth.
B) Ohmic Contacts:	4-Patterning top contact by lift-off method: a) Using mask 2 and negative photoresist to pattern 3 by 3 contacts. b) Metal evaporation Ge-Au/Ge-Ni-Au. c) Removing extra metal.
C) Etching:	5-Chemical etching to isolate devices: a) Photolithography using mask1. b) Chemical etching for a thickness of greater than 1 μm.
D) Isolation Layer:	6-SiO2 deposition by PE-CVD. 7-Patterning SiO2 to open 3 by 3 windows, using mask 2.
E) Metal Contacts:	8-Top contact deposition and patterning by lift-off (mask 3) Ti-Pt-Au. 9-Wafer thinning. 10-Bottom contact deposition Ge-Au/Ge-Ni-Au. 11-Making ohmic contacts by annealing @ 400C for 30 seconds. 12-Cleaving.

Table 4.1. List of major fabrication process steps.

Step 4-a:

In order to be able to pattern metal contacts on wafer through the lift-off technique, the thickness of photoresist must be greater than the thickness of deposited metal. Therefore for this step we used Shipley AZ 1375 negative photoresist.

Spinning: 4500 RPM for 30 seconds.
Prebake: 30 min. @ 90 °C.
Exposure time: 45 sec. using mask aligner Karl Suss MJB3 (mask 2).
Developing: MF 321 for 1 min.
Postbake: 30 min @ 120 °C.

Step 4-b:

The metal was deposited on top of the patterned photoresist by E-beam metal deposition (CHA Industries) at a pressure below 10^{-6} Torr.

Ge: 200 Å
Au/Ge: 800 Å
Ni: 300 Å
Au: 1000 Å

Step 4-c:

By placing the wafer in acetone and using of ultra-sound agitation the extra metal from the surface of wafer was lifted (2 min.).

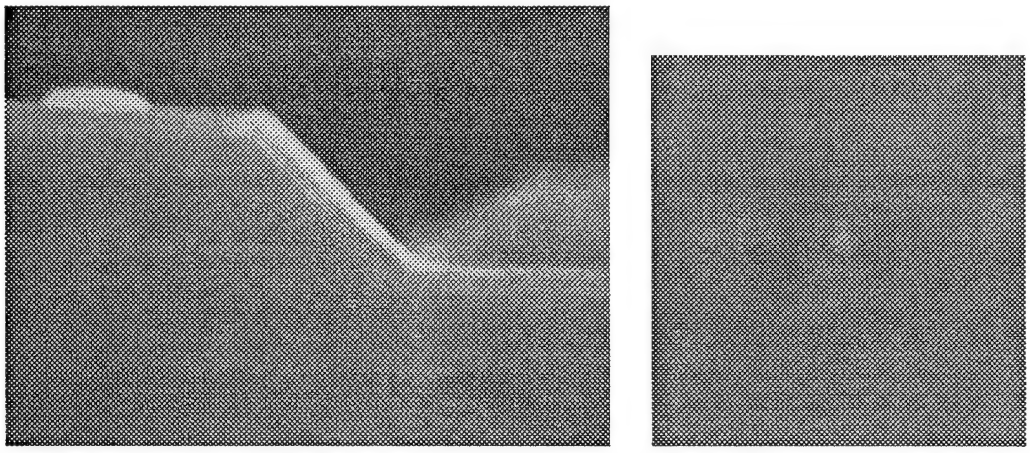
Step 5-a:

Shipley AZ 1805 negative photoresist was used as the mask for mesa definition during the wet etching process. Mask 1 (Appendix B-1) was used to pattern the photoresist.

Spinning: 5000 RPM for 30 seconds.
Prebake: 30 min. @ 90 °C.
Exposure time: 2.7 sec (mask 1).
Developing: MF 321 for 45 sec.
Postbake: 30 min @ 120 °C.

Step 5-b:

Isolated mesa structures were formed by the wet etching process using $H_3PO_4/H_2O_2/H_2O$ (5:1:1) solution. The mesas were etched as high as 1 μm at a rate of 4000 Å/min at 9 °C. Figures 4.6-a and b show the SEM cross section of the structure and top view of a mesa with contact metal on it.



(a) (b)

Fig. 4.6. a) A SEM cross-sectional and b) top view of the etched structures (height of test structure: 6000 Å).

Step 6:

Through Plasma Enhanced Chemical Vapor Deposition (PE-CVD) (Waf'r/Batch Plasma-Therm 70 series system), a 1000Å-thick layer of SiO_2 was deposited on the structures.

Pressure: 900 mTorr.
Temperature: 250 °C.

Step 7:

In order to open windows in SiO_2 layer, Shipley AZ 1813 negative photoresist was used which is thick enough to cover the mesas and forms a planar surface proper for photolithography.

Spinning: 4000 RPM for 30 seconds.
Prebake: 30 min. @ 90 °C.
Exposure time: 7 sec (mask 2).
Developing: MF 321 for 1 min.
Postbake: 30 min @ 120 °C.

Step 8:

The second layer of top metal was deposited by e-beam metal deposition and patterned by lift-off (mask 3).

Ti: 500 Å
Pt: 600 Å
Au: 1000 Å

Step 9:

In order to facilitate cleaving the wafer into devices, it was thinned to 150 μm by mechanical lapping (LOGITECH PM2A machine and 3 μm Aluminum Oxide powder).

Step 10:

Deposition of bottom contact: The same as step 4-b.

Ge: 200 Å
Au/Ge: 1000 Å
Ni: 300 Å
Au: 3000 Å

Step 11:

By Rapid Thermal Annealing (RTA), the contacts were alloyed at 400 °C for 30 seconds which is short enough not to damage the grown structure.

Chapter 5: Results

Figure 5.1 shows the current density versus voltage characteristic of a nominally 7×7 μm^2 device measured by Tektronix 571 curve tracer at room temperature. However, due to etch undercutting during fabrication (~1 μm), the actual area of the resonant tunneling diode is 6×6 μm^2.

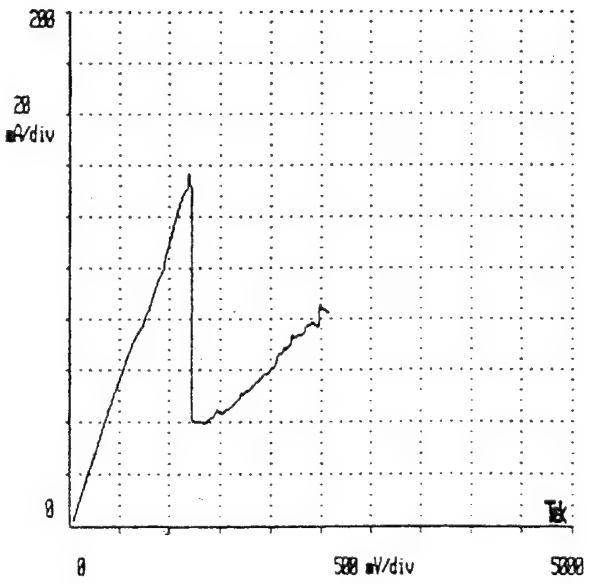


Fig. 5.1. I-V characteristic of a 6×6 μm^2 device based on resonant tunneling through the second energy level.

The peak current density of the device exceeds 300 kA/cm^2 which according to the best of our knowledge is more than 2 times higher than the PCD values reported for GaAs-based RTD's [12], and more than 3 times higher than the PCD's obtained for any type of MOCVD grown RTD's [13]. The peak voltage is around 1.2, volts which could be reduced to less than 1 volt by increasing the well width to 62 Å.

The relatively good peak-to-valley ratio of the device (3:1) at room temperature may be attributed to the following factors:

a) As explained in section 4.1, in order to improve the quantum well interfacial morphology, RTD structures were grown on nominally exact (100) $\pm$ 0.1° GaAs substrate. It is well known that the interface roughness scattering process is one of the major mechanisms contributing to valley current [16], and hence, smooth interfaces between the strained-layer quantum well and barriers are quite essential to ensuring device performance [21].

b) The series resistance has a destructive effect on the negative differential resistance of the device. We achieved good ohmic contacts at the emitter side by using a two-step process as explained in section 4.2.

c) It has been reported that the use of a deep quantum well improves the PVR [22]; however, there are other reports that do not agree with this conclusion [23].

The thermal stability of the device can be improved by increasing the width of well. For example, for a structure with 63Å-wide well the peak voltage reduces to less than 1 volt and the peak current density is also reduced by a factor of 1.5; in turn, the power dissipation in the device is reduced by a factor of 2.

Based on the peak current density and peak voltage of this device (spacer layer=300 Å), and assuming that the associated parasitic capacitance is negligible, the device could switch 1 volt in less than 3 picoseconds [5]. Also by using a pulsed doping layer sandwiched between two undoped layers [8], the intrinsic capacitance of the device can be reduced, which in turn reduces the switching time by a factor of 2 or more. In turn, sub-picosecond switching speed becomes possible.

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